A 5 to 27 GHz MMIC POWER AMPLIFIER.

Kye-Ik Jeon, Jae-Hak Lee , Seung-Won Paek, Dong-Wook Kim, Won-Sang Lee, Chae-Rok Lim, Ho-young Cha, Hyung-kyu Choi, Ki-Woong Chung

RF Device Team, LG Corporate Institute of Technology
16 Woomyeon-Dong, Seocho-Gu 137-724 Seoul, Korea

ABSTRACT

A record of wideband 5 to 27 GHz power amplifier is achieved with 20 dB gain and 21 dBm output power in two stage monolithic form based on LGCIT's 0.25 μm pHEMT. In design, we use lossy matching technique to obtain flat gain characteristic and use Cripps' matching technique to obtain flat output power characteristic. The chip size is compact 3.1 mm x 1.2 mm. We present how to realize wideband output, input and interstage matching network

INTRODUCTION

There have been many needs for wideband power amplifier in microwave system area. For example, EW radar and jammer system designers want to stretch out the covering frequency. Measurement system designers want their system to have wider dynamic range and wider frequency range. They also anticipate that the amplifier has flat gain and flat power characteristic.

Conventionally power amplifier designers have relied on one of two approaches. One is load-pull technique. This technique requires elaborated measurement system which is very difficult to realize in millimeter wave frequencies. The other one is large signal model based approach. The non-linear model with harmonic balance simulator has helped them predict non-linear behavior such as power saturation and efficiencies. However, it needs considerable too much computing time to adopt optimization engine in modern circuit simulator.

In this paper, we present a design method for wideband power amplifier using HEMTs or MESFETs. This method does require just a small signal equivalent circuit model for FET and I-V curves not a rigorous large signal model. This is explained in following section while describing design technique of 130 mW MMIC power amplifier operating form 5 to 27 GHz with flat gain and flat compressed power characteristic.

AMPLIFIER DESIGN

The amplifier design starts with equivalent circuit model and I-V curve of FET to be used. The first step is determining load impedance and output matching network. The optimum load impedance is determined by the dynamic load line of maximized voltage sweep and current sweep in transistor I-V curve. This is called Cripps' method[1]. We found that 40 Ω is output load for maximum power output for our 0.25 x 600 μm GaAs/AlGaAs/InGaAs pHEMT with associated output power of more than 20 dBm.

0-7803-5687-X/00/$10.00 © 2000 IEEE

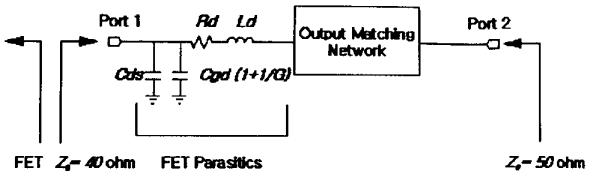

Fig 1 Simplified form of output matching network.

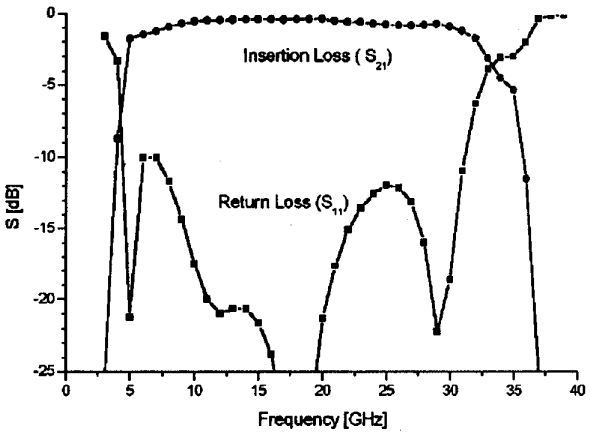

Fig 2 Insertion loss and return loss of output matching network including FET parasitics. Note that the reference impedance is 40 for port1 Ω and 50 Ω for port 2.

What is left for determining output network is 'letting the device see 40 Ω in desired frequency band'. To realize this, we employed band pass transformer that converts this optimum load impedance into 50 Ω. This network includes bias path for drain current and parasitics in FET. Simplified output network is shown in Fig 1. The included parasitic elements are drain access resistance R_{ds}, drain-to-source capacitance C_{ds} and gate-to-drain Miller's capacitor which expressed as $C_{gd}(1+1/G)$, where G is output stage gain. These parasitics are treated as external passive elements those constitute band pass network. They are separately fabricated and on-wafer tested. The measured characteristics are plotted in Fig 2. In this figure, the reference impedance is 40 Ω for port 1 and 50 Ω for port 2. Low return loss means that the current source in transistor's equivalent circuit sees resistive loading of 40 Ω and flat insertion loss implies flat power characteristic. These two curves say that the transistor delivers maximum power it can generate to output load with flat frequency characteristic in 5-30 GHz band.

To obtain flat gain characteristic we used lossy matching technique [2] in input and interstage matching circuits that are made of band-pass section blended with lossy resistor. As illustrated in Fig 3, shunt connection of series *RL* and series connection of parallel *RC* circuits are used. Element values of these high pass networks are optimized in order to compensate 6 dB unilateral gain slope of common source FET by absorbing lower band power. When we design interstage circuit, as we did in output matching circuit, the S_{11} of 2nd stage FET is transformed so as to make current source of 1st stage 600 μm pHEMT see around 40 Ω. This makes 1st stage transistor deliver enough power to drive 2nd stage therefore avoids earlier saturation of the amplifier.

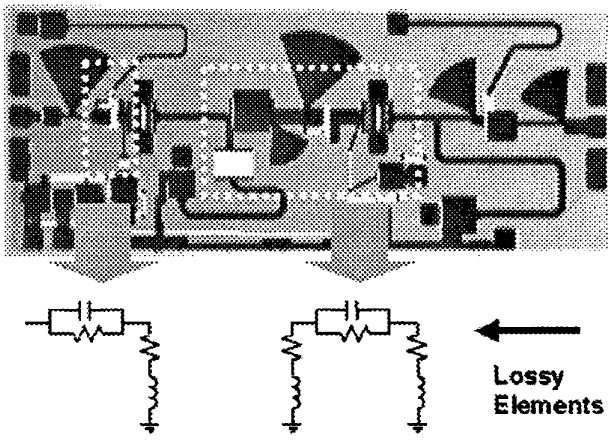

Fig. 3 Photograph of fabricated power amplifier. Lossy matching circuit is indicated in simplified form.

The device is biased at drain voltage of 4.4 V with a current of 90 mA for each stage. The simulated amplifier performance is presented in Fig 4. To obtain compactness lumped MIM capacitor is used than open stub for shunt susceptance element. However radial stubs are used instead when we need shunt capacitor less than 0.2 pF to maintain accuracy. The chip size is 1.2mm × 3.1mm with substrate thickness of 100 μm.

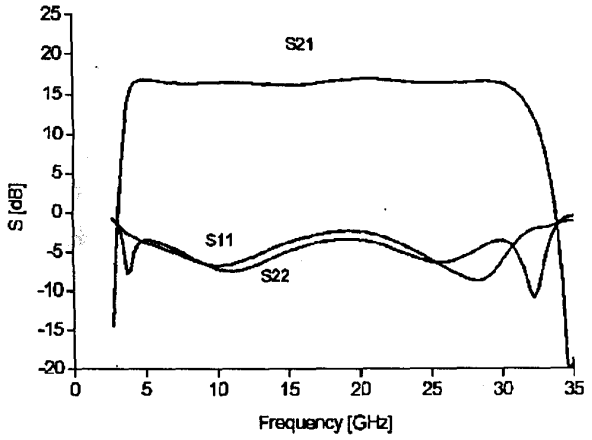

Fig. 4 Simulated small signal characteristic of 2stage wideband power amplifier

AMPLIFIER PERFORMANCE

The MMIC amplifier is tested on wafer. Fig 5 shows the measured scattering parameters of the amplifier. This graph shows small signal gain of 20 ± 1.7 dB at the frequency range of 4.5 to 27 GHz. The bias is 4.4 V and the drain current is 90 mA per each stage. At the same bias, P_{out}-P_{in} is measured at 5, 14, 24 and 26.5 GHz and presented in Fig 6. This graph shows 21 dBm saturated power. We see that small signal flatness conserved also in saturated power characteristic.

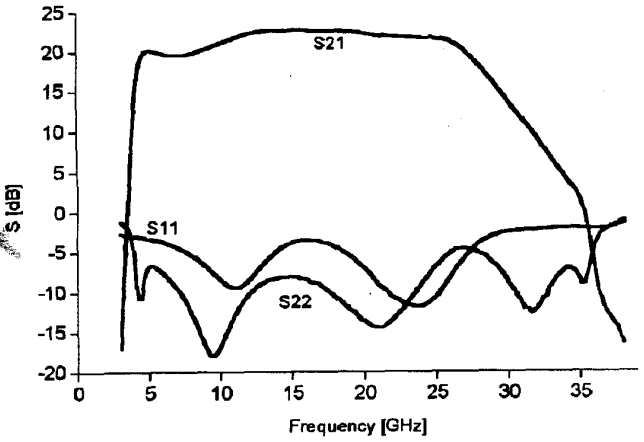

Fig. 5 Measured small signal characteristic of 2 stage wideband power amplifier

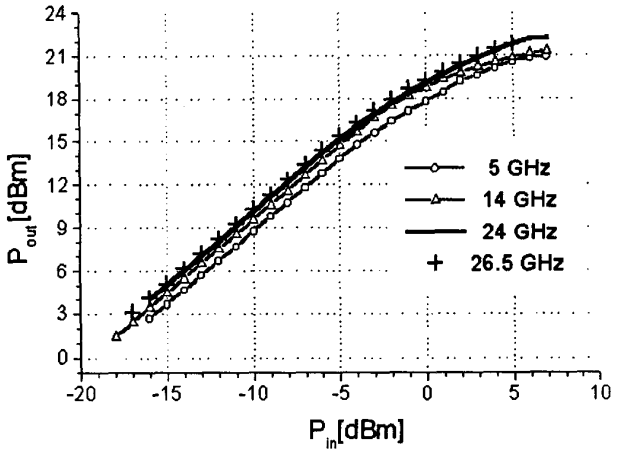

Fig . 6 Measured P_{out}-P_{in} characteristic at 5, 14, 24 and 26.5 GHz.

CONCLUSIONS

A wideband power amplifier using 0.25 μm GaAs/AlGaAs/InGaAs pHEMT is demonstrated. This amplifier operates at 5 to 27 GHz with output power of 21 dBm. Lossy matching circuits blended with band pass networks are used in interstage and input networks to achieve flat small signal gain characteristic. We used the

band pass impedance transformer in output matching circuit to obtain flat output power saturation characteristic.

ACKNOWLEDGMENT

The authors would like to thank Jin-Wook Shin and Jong-Won Lee for their efforts in MMIC process. The authors also would like to thank Kyung-Hak Lee for his support during measurement.

REFERENCES

[1] Steve C. Cripps, "RF Power Amplifiers for Wireless Communications," Artech House 1999, Chapter 2

[2] George D. Vendelin, Anthony M. Pavio, Ulrich L. Rohde, "Microwave Circuit Design," John Wiley & Sons, 1990, Chapter 5, pp. 347