1-26 GHZ HIGH POWER P-I-N DIODE SWITCH

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ABSTRACT

Wide-band high power GaAs p-i-n diode SPDT switch is presented. Insertion loss is less than 0.7dB and isolation is better than -38 dB for 1-26 GHz frequency range. Maximum power handling capability is 35dBm at 1.8GHz where the bias voltage is -15 V. Composite buffer layer of superlattice and low temperature grown GaAs prevents the problems of power limitation related with epitaxial buffer layer of p-i-n diode structure.

INTRODUCTION

High power switching device is one of the key elements in communication system and radar system. Vertical epitaxial GaAs p-i-n diode shows high breakdown voltage, fast switching speed, high linearity, and high isolation characteristics, so that it is widely used in high power, wide-band switching circuit[1]-[4].

We designed and fabricated series-shunt type wide-band, high-power SPDT p-i-n diode switch MMIC. Also we report power limitation mechanism by buffer leakage and solution for this problem.

DESIGN

A series-shunt-shunt type switch arm configuration was used to decrease through-loss and to increase isolation. Figure 1 is the schematic of SPDT switch. Transmission line length between two shunt diodes was optimized to obtain high isolation at the high frequency range. The width of transmission line, which is critical for matching of shunt diode at through state, is 30μm to obtain characteristic impedance of 68Ω. The external bias circuit supplies forward bias current of 11mA and reverse bias voltage of −15V.

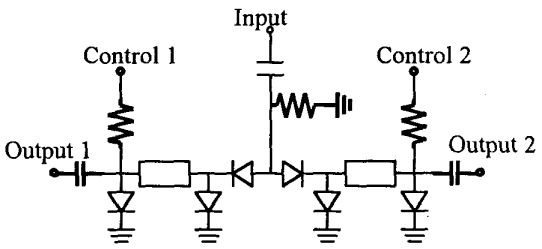

Figure 1 Schematic of SPDT switch.

EXPERIMENTS AND RESULTS

The p-i-n diode structures were grown by molecular beam epitaxy(MBE) on semi-insulating GaAs substrates. The structure of p-i-n diode is as shown in figure 2.

The diode has a 0.5μm thick Be-doped p^+ GaAs layer followed by a 2.5μm thick

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undoped GaAs layer, 1.5μm n^+ GaAs layer, and buffer layer. Wet chemical etching was used to fabricate double mesa structure. Pt/Ti/Pt/Au and AuGe/Ni/Pt/Au metal films were evaporated and alloyed to form p-type and n-type ohmic contact, respectively. Si_3N_4 dielectric film is used for passivation of etched GaAs surface. Front side processing is completed by electroplating of transmission line and air-bridge interconnection. To minimize series inductance and thermal resistance, wafer thinning to 100μm, via-hole etching, backside metallization were performed. Figure 3 shows the photography of SPDT switch MMIC and the size of the chip is 2.5mm x 1.0mm.

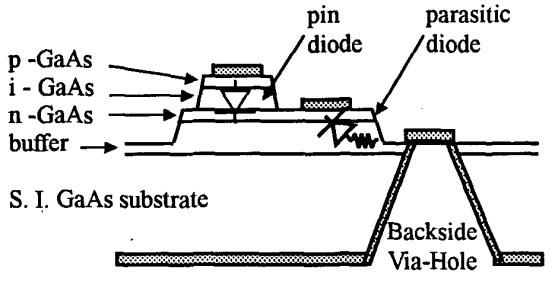

Figure 2 Structure of p-i-n diode.

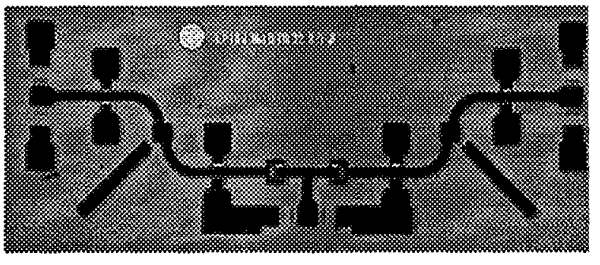

Figure 3 Photography of SPDT switch MMIC. (2.5 mm x 1.0 mm)

Two types of epitaxial buffer layer structure were designed in this study. Buffer type I is composed of 3000Å-thick undoped GaAs layer only. Buffer type II consists of GaAs/AlGaAs super-lattice and low temperature grown GaAs which is known to prevent buffer related back-gating effect in FET structure [5].

As the epi-structures except the buffer are same for both epi-wafers, dc and small signal RF characteristics are almost the same. Forward turn-on voltage is 1.3V and maximum current is about 300mA for the p-i-n diode with 20μm x 20μm anode size. Reverse breakdown voltage is about –65V. Small signal resistance is 1.1Ω at the forward bias current of 10mA and junction capacitance at the reverse bias is about 20fF for 20μm x 20μm diode. The resulting switching cut-off frequency is as high as 6.6THz. Figure 4 is the frequency dependency of small signal insertion loss and isolation of SPDT switch fabricated from epitaxial layer using buffer type II. Insertion loss is less than 0.7dB and isolation is better than -38 dB for 1-26 GHz frequency range.

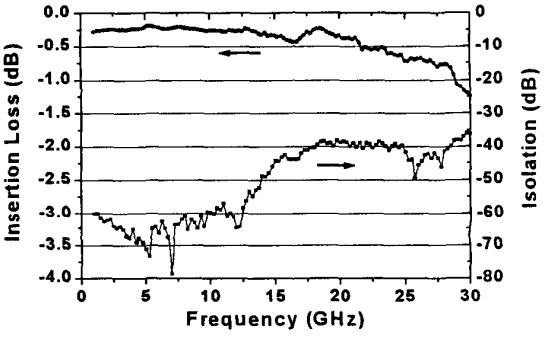

Figure 4 Insertion loss and isolation characteristics of SPDT switch.

We found that the power performance of p-i-n diode is much related with buffer layer structures. Figure 5 is the insertion loss curve at 1.8GHz for the SPDT switch fabricated from epitaxial layer using buffer type I. As the input power increases, insertion loss increases. And at the input power of 29dBm, insertion loss increases dramatically. It can be explained by

leakage current path formation at buffer layer. As undoped GaAs layer grown by MBE is slightly p-type, parasitic diode can be formed between n-type GaAs layer and buffer layer which is in contact with ground plane through back-side via hole as shown in figure 2. In switch circuit, p-i-n diodes are used for series diode and shunt diode. For shunt diode, cathode as well as buffer is always grounded through back-side via hole, that parasitic conduction is not important. However, for series diode, buffer is not connected to either anode or cathode, so that it can be considered as a third electrode. As input power to the switch increases, the signal voltage swing increases, and that parasitic diode between cathode and ground turns-on which leads to the deterioration of insertion loss. The turn-on voltage of parasitic diode is about 14 volts.

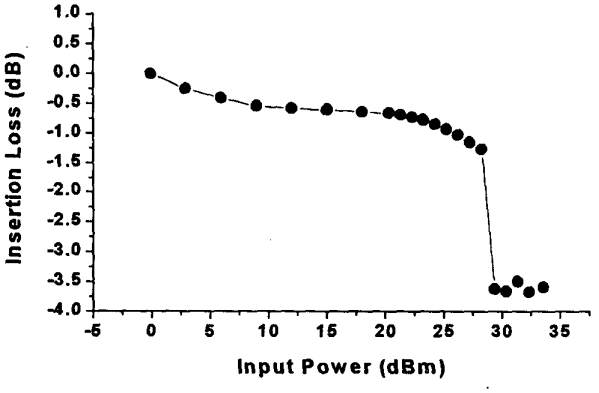

Figure 5 Power characteristic of SPDT switch using buffer structure I at 1.8GHz.

In buffer structure II, low temperature grown GaAs buffer layer suppresses adverse substrate effects and superlattice buffer layer increases potential barrier between n^+ GaAs layer buffer layers which is exposed to surface by mesa etching. Parasitic conduction was not found up to the 100 volts, and that power handling capability is limited by intrinsic properties of p-i-n diode such as reverse breakdown voltage and forward current capability. Figure 6 is the insertion loss and isolation curve at 1.8GHz of SPDT switch using buffer structure II. Insertion loss is less than 0.7dB up to the input power of 35 dBm, which is limited by bias voltage of −15V. Increment of power handling capability is expected by increasing bias voltage and bias current. Almost no change is found for isolation.

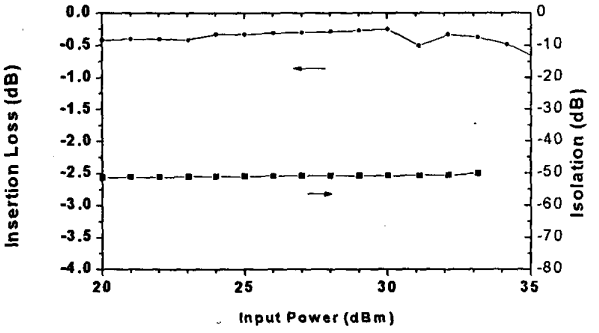

Figure 6 Power characteristic of SPDT switch using buffer structure II at 1.8 GHz.

CONCLUSIONS

GaAs p-i-n diode SPDT switch described here demonstrated excellent characteristics. Insertion loss is less than 0.7dB and isolation is better than 38 dB from 1GHz to 26GHz. The switch is capable of handling input power of 35dBm only with minor change in insertion loss and isolation value. We found buffer related power limitation mechanism in epitaxial layer with thin GaAs buffer and it can be suppressed by using buffer layer structure with superlattice layer and low temperature grown GaAs layer.

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