ULTRA HIGH Q INDUCTOR AND RF INTEGRATED PASSIVE DEVICES ON THICK OXIDE SI SUBSTRATE

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ABSTRACT

Stringent demand to achieve cost and size reduction makes all the companies in the supply chain pursue new technology and apply revolutionary techniques to their products. For this ultimate goal, we developed low cost manufacturing technology for RF substrate and high performance process technology for RF IPDs(Integrated Passive Devices) by electrochemically forming thick oxide layer on Si wafer and using Cu metal and BCB material for metal interconnection and interlayer. The fabricated substrate is 6" Si wafer with 25μm oxide thickness and it showed very good insertion loss of 0.03dB/mm at 4GHz, in case of coplanar transmission line (W=50μm, G=20μm), which included the conductive metal loss. Based on these process technologies, we fabricated ultra high Q inductor on Si, showing the maximum quality factor of 120. To the knowledge of the authors, it is the highest value that has been achieved on Si substrate. Several kinds of RF IPDs with small form factors were also fabricated on thick oxide wafer and they also showed good RF performances in spite of small chip size. These will be widely utilized in hand-held modules and systems where the size or volumetric efficiency is a critical buying criterion.

Key words: thick oxide Si substrate, BCB interlayer, Cu inductor, IPD(Integrated Passive Device)

INTRODUCTION

The technologies that have been widely used in recent wireless market could be categorized into silicon-based semiconductor technology and compound semiconductor technology. The former is based on Si BJT, Si CMOS and SiGe BICMOS [1]-[3] and the latter includes GaAs MESFET, GaAs HBT, GaAs HEMT and InP HBT utilized to implement commercial wireless RF integrated circuits and millimeter wave integrated circuits for military, space, and broadband communications [4]-[6]. Silicon substrate is known to have a lot of benefits of cheap material, good thermal conductivity and stable and mature process technology. But its utilization has been limited in fast growing wireless market by large signal loss and signal leakage through parasitic substrate capacitance in high frequency region. On the other hand, compound semiconductor provides very good microwave performance and has been widely used in fabricating commercial RF integrated circuits. However, it is very expensive, which should be resolved through continual research and development to survive in keen competition of the market.

There have been tried many methods so that Si substrate can be used as cheap substrate for RF and microwave applications. They are including a method to control doping density to make Si substrate have high resistivity in high frequency region [7], a method to form 9μm SiO_2 layer on Si substrate [8], a method to coat 10μm polyimide layer on Si substrate [9], and so on. But all these approaches did not provide remarkable benefits in terms of cost effectiveness and microwave performance.

Conventionally the insulating property of SiO_2 layer is used for isolation, and effective operation of this SiO_2 layer in RF applications requires it to be thick, in order to capacitively isolate it from the underlying conducting Si substrate. In consideration of the economic and manufacturing factors, new method to reduce the fabrication costs and the time required to grow thick oxide is required, and so porous silicon technique is considered as a potential solution. In porous material, the lattice has a large number of its silicon atoms removed by an electrochemical reaction, producing honeycomb-like structure. Initial work on using porous silicon for RF applications took advantage of the oxidation process of the porous silicon layer [10]. More recently, the highly

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insulating nature of porous silicon was used to alleviate the stresses generated as a result of the difference in thermal expansion coefficients of the oxidized porous layer and Si substrate [11]. All of these attempts were done in university laboratories and their RF performances were not fully optimized partially because of their semiconductor processes.

In this paper, we will provide improved Si substrate technology, called Si smart substrate or TO(Thick Oxide) Si substrate, and Cu process with BCB(Benzo Cyclo Butene) interlayer for low cost manufacturing process and good RF performance, compared to conventional approaches. And the performances of the fabricated inductors and several IPDs on thick oxide Si substrate will be also provided for wireless hand-held applications.

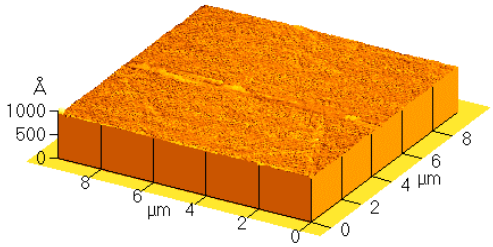
Si SMART SUBSTRATE

Unlike semi-insulating GaAs or InP, silicon has typically been forced to rely upon the insulating properties of SiO_2 for isolation. There requires very thick oxide layer to isolate capacitively between devices on Si substrate. The challenge to implement thick oxide layer is two-fold. One is silicon substrate shattering due to the difference in thermal expansion coefficients of the oxide layer and Si substrate. The other is cost-effective manufacturing. Basically the fabrication cost and the time to grow such thick oxide by conventional techniques make the implementation unrealistic. To overcome the limitations of the conventional techniques, we used 6 inch oxidized porous silicon technique, which is typically formed in an electrochemical cell using HF solution and anodization technique.

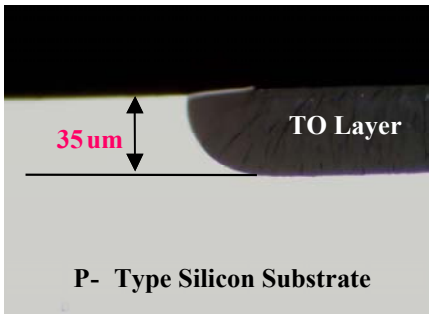
Uniform oxide layer of 25μm or greater was made on the whole surface of 6" silicon wafer. The thick oxide layer can be also made selectively through thin dielectric masking process. The thick oxide Si substrate is called Si smart substrate, though it was also named as OPS(Oxidized Porous Silicon) or SOPS(Selectively Oxidized Porous Silicon) before [10]. Currently, maximum oxide thickness of 6" wafer is 35μm but reproducible and reliable oxide thickness is 25μm, which will be improved continually. The time to make this 25μm oxide layer is less than half an hour. The record oxide thickness and processing time lead to a revolutionary low loss and low cost solution for RF and microwave thin film substrate.

Fig. 1 shows the photograph of 6" 35μm thick oxide silicon wafer. This oxide wafer is very flat (below 18Å) enough to make fine features of ~1μm. The AFM(Atomic Force Microscope) image is shown in figure 2(a). Figure 2(b) shows the cross sectional SEM(Scanning Electron Microscope) image of thick oxide wafer. The thick oxide layer was be formed selectively using thin dielectric layer masking, as shown in figure 2(b). To make the most of Si smart substrate for RF applications, we developed passive integration process using Cu metallization and BCB interlayer. This process will be explained in next section. The insertion loss of fabricated coplanar transmission line (W=50μm, G=20μm) on Si smart substrate of 25μm oxide thickness showed 0.03dB/mm at 4GHz, including conductive metal loss. Especially, the transmission line showed high performance up to more than 10GHz. The insertion loss was below 0.1dB/mm up to 15GHz. It was superior to that of expensive HRS(High Resistivity Silicon, 7Kohm-cm) substrate and comparable to that of glass substrate. Table 1 shows the comparison data of the transmission line losses obtained from this work and other research results.

Figure 1. The photograph of 6" thick oxide silicon wafer (SiO_2 layer thickness = 35μm)



(a)



(b)

Figure 2. Surface roughness and cross sectional view of thick oxide wafer : (a) AFM image : surface roughness ≤ 18Å @10μm×10μm (b) cross sectional SEM image of the wafer

Insertion loss (dB/mm)	Dielectric material & thickness	Signal line metal	Substrate	Ref.
0.17 @ 4GHz	SiO_2 (0.9μm)	Al (1μm)	HRS (4KΩ-cm)	IEEE EDL 1991
0.19 @ 4GHz	Polyimide (10μm)	Al (4μm)	Silicon (20Ω-cm)	IEDM 1995
0.2 @ 4GHz	-	Al (1.25μm)	HRS (10KΩ-cm)	IEEE MGWL 1999
0.1 @10GHz	SiO2 (0.1μm) Polysilicon (0.6μm)	Al (1μm)	HRS (10KΩ-cm)	IEEE MGWL 1999
0.05 @ 4GHz	-	Au (5μm)	Pyrex	Exp. data
0.03 @ 4GHz	**thick oxide (25μm)**	**Cu (10μm)**	**Silicon (8Ω-cm)**	**This work**

Table 1. The insertion loss comparisons of coplanar transmission lines obtained from this work and other research results.

LOW COST AND HIGH PERFORMANCE RF PASSIVE MANUFACTURING PROCESS

To achieve low cost and high performance manufacturing process, we developed Cu-BCB passive process. Cu metal is optimal choice for low conductive metal loss and high-speed operation in tough environment. We used 10μm Cu plating process for low loss inductor fabrication and interconnection. For resistor, NiCr was used and TaN is currently under development. SiN_x dielectric material was employed as interlayer insulator of MIM(Metal-Insulator-Metal) capacitor. Total two Cu metal layers and one dummy Cu layer were used. The dummy metal layer was used for the definition of top metal of MIM capacitor. Between the remaining two metal layers, one was for NiCr metal contact, bottom metal of MIM capacitor and interconnection between inner part and outer part of spiral inductor, and the other was for top metal of MIM capacitor, spiral inductor patterning and interconnection.

Photosensitive BCB material was used as interlayer between first Cu metal and Cu plating metal in this work. Photo-BCB had been originally developed for use in microelectronics applications, including Multi Chip Module(MCM) and flat panel display. Because the photo-BCB has many attractive properties such as processing compatibility with existing IC manufacturing techniques, low moisture uptake, low cure temperature, rapid thermal curing, high planarization level, low dielectric constant and so on, it was adopted in our process. The BCB layer of 4.5μm was used for interlayer of metal layers and the BCB layer of 3μm was used for final passivation.

The process flow is as follows. In the first place, Si wafer with thick oxide(25μm) is prepared. And then the SiN_x layer is deposited on whole front side of the wafer to stabilize the microstructure. NiCr is deposited and patterned by lift-off process for thin film resistor. Ti/Cu metal evaporation for NiCr contact is followed by SiN_x dielectric material deposition for MIM capacitor. Etching process forms the dielectric via and dummy Ti/Cu metal is evaporated to define the top area of MIM capacitor. BCB layer is coated on wafer and BCB via process is performed. Then 10μm Cu plating process and BCB passivation process is performed. Pads are finally opened by BCB etching process. Depending on the applications, final Ni/Au treatment can be done.

Figure 3 shows schematic cross sectional view of pad structure by this process. The developed Cu-BCB process is low cost manufacturing process, compared to Au process typically used in III-V compound industry and is high performance process due to low loss characteristics of Cu and BCB for RF applications, compared to Al process widely used in Si based semiconductor industry. Therefore this is very optimal process for high quality RF passive integration.

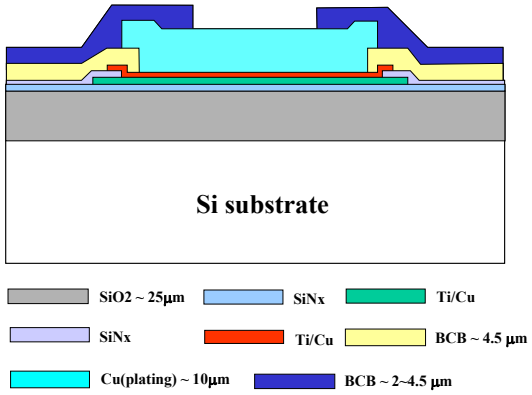


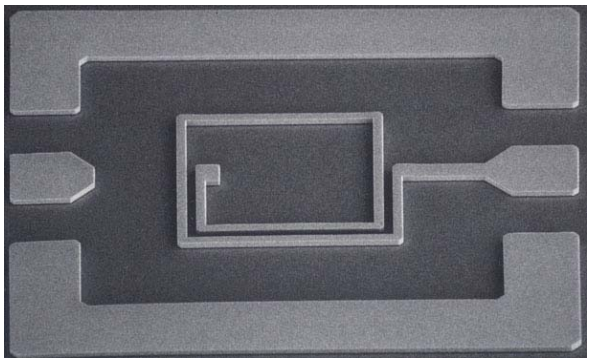
Figure 3. Cross sectional view of pad metal structure

HIGH Q INDUCTOR ON Si SMART SUBSTRATE

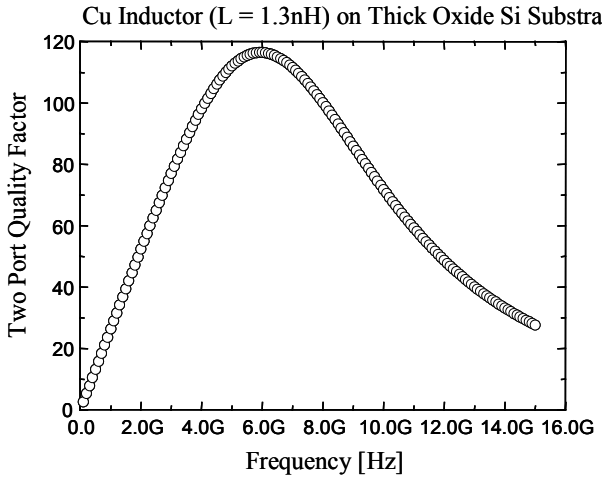
We resolved one of the major technological challenges in fabricating RF integrated circuit on Si substrate, on-chip inductor implementation, by using low cost porous silicon process and advanced oxidization process to make very thick SiO_2 layer. As mentioned in previous section, to improve inductor performance, BCB interlayer technology and Cu plating technology were used together with our developed thick oxide substrate technology. The on-chip inductors were fabricated with Cu thickness of 10μm on 25μm thick oxide 6" silicon wafer. Small size spiral inductor of 1.3nH with 10μm line and spacing showed the maximum quality factor of ~120 at 6GHz, which, to the knowledge of the authors, is the highest value on Si substrate in the world. The fabricated on-chip inductors showed the maximum quality factor range of 30~120, depending on geometrical factors and inductance

values of 0.6~35nH. Especially the inductors showed high quality factors in broadband frequency range. For example, the quality factor of 1.3nH Cu spiral inductor was more than 40 up to 12GHz and maximum quality factor was about 120 at 6GHz. The SEM photograph of the fabricated Cu inductor and two-port quality factor extracted from the measured data are shown in figure 4. These thick oxide substrate technology and high Q inductor technology have the potential not only to push the RF operating window for Si MMICs well into the 10GHz range but also to broaden the area of IPDs, which has been limited to low frequency region of several hundred MHz, up to 10GHz or above.

Figure 5 shows the maximum quality factor distribution with inductance values. In case of inductance values less than 10nH that are commonly used in RFICs, the maximum quality factors have the values more than 50. As shown in figure, the different maximum quality factors and different frequency characteristics are obtained from different geometries, although they have very similar inductance values. Therefore, the circuit designers should choose proper inductors for their specific applications.



(a)



(b)

Figure 4. The photograph and the two-port quality factor extracted from the measured results of 1.3nH Cu inductor

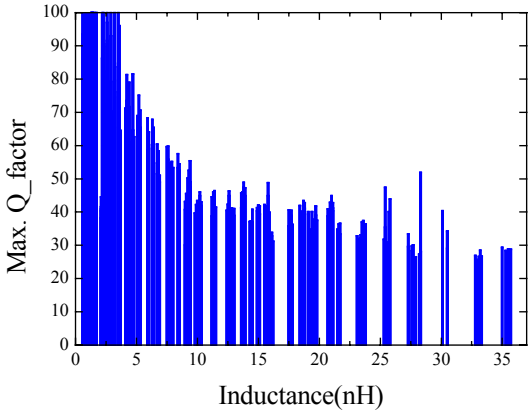


Figure 5. Maximum quality factor distribution with inductance values of 10μm rectangular Cu inductors

RF INTEGRATED PASSIVE DEVICES

MIM capacitors and NiCr thin film resistors for RF applications can be also integrated on thick oxide substrate, because of its extremely flat surface. These thick oxide substrate technology and RF passive integration technology of MIM capacitors, resistors, high Q inductors enable to push the RF capability of Si wafer well into 10GHz range, offering real competition in a regime that they consider the exclusive domain of GaAs and InP. Utilizing high quality passive devices, we fabricated several IPDs such as low pass filter, power combiner, fixed attenuator, balun and etc. These devices could be wafer-level-packaged using PbSn solder ball bumping of 290μm diameter for very small form factor and be packaged in SMT(Surface Mounting Technology)-compatible LGA(Land Grid Array) body or equivalents.

Figure 6 shows the fabricated LC-type lumped balun as an example. Balun layout was configured for wafer level packaging and its size was 1.75mm×1.75mm. In case of balun for wire bonding in the module, the size can be decreased to be 2.0mm^2 or less. Figure 7 shows RF performances of 1700MHz LC-type lumped balun that was fabricated on thick oxide wafer using 10μm Cu plating process. At 1700MHz, the insertion loss of the balun was about 0.9dB and amplitude and phase imbalances were less than 0.1dB and 2^o, respectively. In case of 900MHz and 1800MHz power combiners, the insertion loss was about 0.7dB, the return loss was less than –15dB, and port isolation was greater than 20dB. Four fixed attenuators were implemented on the size of 2mm×2mm for wafer level packaging using solder ball bumping. Π-type circuit topology was employed and the attenuation level was constant up to 3.5GHz. All the VSWRs(Voltage Standing Wave Ratio) were less than 1.3, although they were depending on the attenuation levels. In case of low pass filter, our conventional process can obtain the insertion loss of 0.5dB with harmonic

attenuation of more than 30dB. Cu-based low pass filter has much superior current handling capability to Au-based filter and Al-based filter widely used in Si MMIC industry or GaAs MMIC industry. Although the fabricated IPDs were not fully optimized in terms of circuit topology and remained to be improved, low cost microwave passive devices with small form factor that showed good performances in microwave region were successfully fabricated and evaluated on 6" silicon wafer with our new technology. These IPDs will be the optimal solution for hand-held modules and systems where the size or volumetric efficiency is a critical buying criterion.

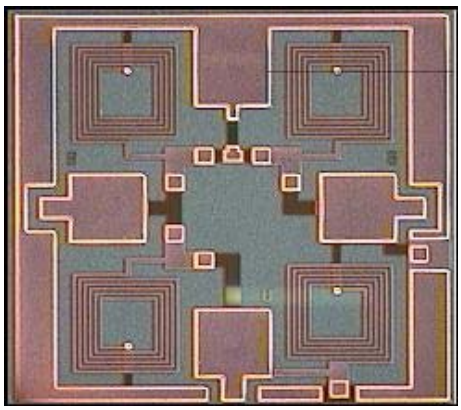
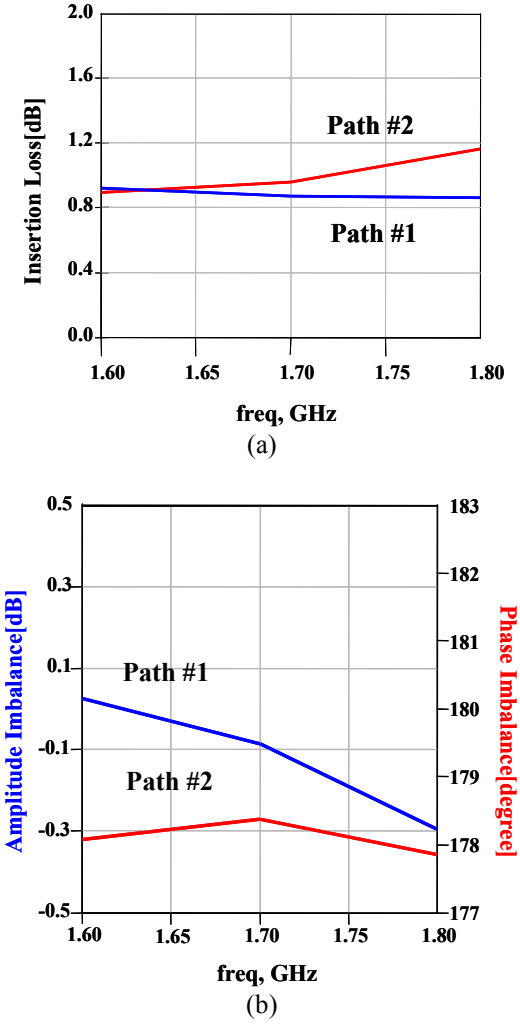


Figure 6. The photograph of the LC-type lumped balun

CONCLUSIONS

The requirement of the cost and size reduction push all the companies in the supply chain to find new solutions out for their product competence. Up to now, there have been many researches on RF passive integration on Si wafer for low cost and mass-producible process. However, they have not provided satisfactory solutions and the results were not be utilized in commercial industry. Based on this industry demand, we have developed low cost manufacturing technology for RF substrate and high performance passive process technology for RF IPDs by forming thick oxide on Si wafer and using Cu metal and BCB interlayer material. The fabricated substrate of 25μm oxide thickness showed good insertion loss of 0.03dB/mm at 4GHz, in case of coplanar transmission line with W=50μm and G=20μm, which included the conductive metal loss. Especially the transmission line showed high performance up to more than 10GHz. The insertion loss was below 0.1dB/mm up to 15GHz. It was much superior to that of expensive HRS(High Resistivity Silicon, 7Kohm-cm) substrate. With these well-developed processes, we achieved ultra high Q inductor on Si wafer, which showed the maximum Q factor of 120. To the knowledge of the authors, it is the highest value on Si substrate in the world. The fabricated on-chip inductors showed the maximum quality factor range of 30~120, depending on geometrical factors and inductance values of 0.6~35nH. Especially the inductors showed high quality factors in broadband frequency range. For example, the quality factor of 1.3nH Cu spiral inductor is more than 40 up to 12GHz and maximum quality factor is about 120 at 6GHz. We fabricated RF IPDs with small form factor. They showed good RF performances in spite of small chip size.



Path #1: unbalanced port to balanced port 1
Path #2: unbalanced port to balanced port 2

Figure 7. RF performances of 1700MHz LC-type lumped balun fabricated on thick oxide wafer: (a) insertion loss (b) amplitude and phase imbalances

These thick oxide technology and high quality RF passive integration technology of MIM capacitors, resistors and high Q inductors have the potential to push the RF operating window for Si wafer well into the 10GHz, offering real and keen competition in a regime that they consider the exclusive domain of GaAs and InP. And also these will broaden the area of IPDs, which has been limited to lower frequency region of several hundred MHz, up to more than 10GHz. Finally the developed

technologies in this paper will be widely utilized in hand-held modules and systems where the size or volumetric efficiency is a critical buying criterion.

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