High Quality RF Passive Integration using 35μm Thick Oxide Manufacturing Technology

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Abstract

The strong pressure of cost and size reduction in wireless industry makes the phone makers find new and revolutionary solutions for their products. Among the various approaches, the passive integration is the most attractive way. To achieve both goals of dramatic size reduction and additional cost reduction, we developed low cost manufacturing technology for RF substrate and high performance process technology for RF integrated passive devices by electrochemically forming thick oxide on Si wafer and using Cu metal and BCB material for metal interconnection and interlayer. The fabricated substrate is conventional 6" Si wafer with SiO_2 thickness of 25μm on the surface. This substrate showed the very good insertion loss of 0.03dB/mm at 4GHz, including conductive metal loss, in case of 50Ω coplanar transmission line (W=50μm, G=20μm), and provided cost-effective solution in RF passive integration. Based on these process technologies, we fabricated ultra high Q inductor on Si, which showed the maximum quality factor of 120. Several RFIPD (Integrated Passive Device) were also fabricated on thick oxide silicon and they showed good RF performances in spite of small chip size. In case of power divider, the insertion loss is below 0.5dB and isolation is more than 25dB. The 900MHz low pass filter has 0.5dB insertion loss and more than 25dB attenuation at second and third harmonics. These will be widely utilized in hand-held module and system where the size or volumetric efficiency is a critical buying criterion.

Key words: thick oxide Si substrate, BCB interlayer, Cu inductor, integrated passive device

Introduction

The technologies that have been widely used in recent wireless market could be categorized into silicon-based semiconductor technology and compound semiconductor technology. The former is based on Si BJT, Si CMOS and SiGe BICMOS [1]-[3] and the latter includes GaAs MESFET, GaAs HBT, GaAs HEMT and InP HBT utilized to implement commercial wireless RF integrated circuits and millimeter wave integrated circuits for military, space, and broadband communications [4]-[6]. Silicon substrate is known to have a lot of benefits of cheap material, good thermal conductivity and stable and mature process technology. But its utilization has been limited in fast growing wireless market by large signal loss and signal leakage through parasitic substrate capacitance. There have been tried many methods so that Si substrate can be used as cheap substrate for RF and microwave applications. They are including a method to control doping density to make Si substrate have high resistivity in high frequency region [7], a method to form 9μm SiO_2 layer on Si substrate [8], a method to coat 10μm polyimide layer on Si substrate [9], and so on. But all these approaches did not provide remarkable benefits in terms of cost effectiveness and microwave performance.

Conventionally the insulating property of SiO_2 layer is used for isolation, and effective operation of this SiO_2 layer in RF applications requires it to be thick, in order to capacitively isolate it from the underlying conducting Si substrate. Based on economic and manufacturing considerations, new method to reduce the fabrication costs and the time required to grow thick oxides is required, and so porous silicon technique is considered as a potential solution. In porous material, the lattice has a large number of its silicon atoms removed by an electrochemical reaction, producing honeycomb-like structure. Initial work on using porous silicon for RF applications took advantage of the oxidation process of the porous silicon layer [10]. More recently, the highly insulating nature of porous silicon was used to alleviate the stresses generated as a result of the difference in thermal expansion coefficients of the oxidized SiO_2 and Si substrate [11]. All of these tries were done in university laboratories and their RF performances were not fully optimized by using their semiconductor processes.

In this paper, we will introduce improved Si substrate technology, called Si smart substrate or TO(Thick Oxide) Si substrate, and Cu process with BCB(Benzo Cyclo Butene) interlayer for low cost manufacturing process and high RF performance, compared to conventional approaches. And the performances of the fabricated inductors and several kinds of integrated passive devices on thick oxide Si substrate will be also provided for wireless hand-held applications.

Substrate

There requires very thick oxide layer to isolate capacitively between devices on Si substrate. The challenge to implement thick oxide layer is two-fold. One is silicon substrate shattering due to the difference in thermal expansion coefficients of the oxide layer and Si substrate. The other is processing time to obtain thick oxide. Basically the fabrication costs and the time to grow such thick oxide by conventional techniques make the implementation unrealistic. To overcome the limitations of the conventional techniques, we used oxidized porous silicon, which is typically formed in an electrochemical cell using HF solution and anodization technique.

Uniform oxide layer of 25μm or greater was made on the whole surface of 6" silicon wafer. The thick oxide layer can be also made selectively through dielectric masking process. The thick oxide Si substrate is called Si smart substrate, though it was also named as SOPS(Selectively Oxidized Porous Silicon) before [10]. The time to make this 25μm oxide layer is less than half an hour. The record oxide thickness and the processing time lead to a revolutionary low loss and low cost solution for RF and microwave thin film substrate.

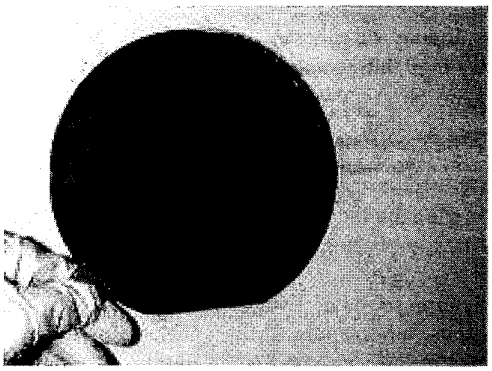
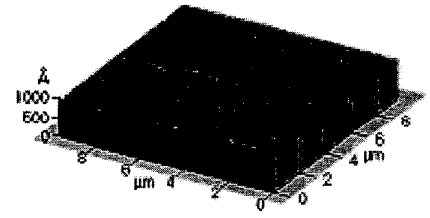
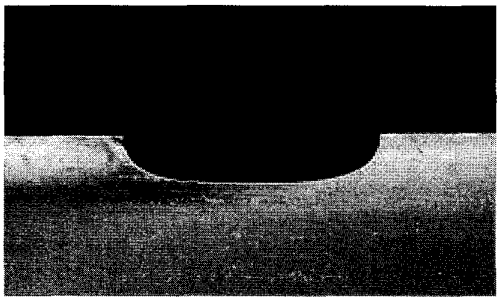


Figure 1. The photograph of 6" thick oxide silicon wafer (SiO_2 layer thickness = 35μm)

Fig. 1 shows the photograph of 6" 35μm thick oxide silicon wafer. This oxide wafer is very flat (below 18Å) enough to make fine features of ~1μm.



(a)



(b)

Figure 2. Surface roughness and cross sectional view of thick oxide wafer : (a) AFM image : surface roughness ≤ 18Å @10μm×10μm (b) cross sectional SEM image of the wafer

The AFM(Atomic Force Microscope) image is shown in figure 2(a). Figure 2(b) shows the cross sectional SEM(Scanning Electron Microscope) image of thick oxide wafer. To make the high performance devices for RF applications, we developed Cu metallization and BCB interlayer process. This process will be explained in next section. The insertion loss of fabricated coplanar transmission line (W=50μm, G=20μm) is 0.03dB/mm at 4GHz, including metal conductive loss. Especially, the transmission line showed high performance up to more than 10GHz. The insertion loss was below 0.1dB/mm up to 15GHz. It was superior to that of expensive HRS(High Resistivity Silicon, 7Kohm-cm) substrate and comparable to that of glass substrate. Table 1 shows the comparison data of coplanar transmission line losses obtained from our work and other research results.

IL (dB/mm)	Dielectric (thickness)	Metal	Substrate	Ref.
0.17 @4GHz	SiO_2 (0.9μm)	Al (1μm)	HRS (4KΩ-cm)	IEEE EDL 1991
0.19 @ 4GHz	Polyimide (10μm)	Al (4μm)	Silicon (20Ω-cm)	IEDM 1995
0.2 @ 4GHz	-	Al (1.25μm)	HRS (10KΩ-m)	IEEE MGWL 1999
0.1 @10GHz	SiO2 (0.1μm) Polysilicon (0.6μm)	Al (1μm)	HRS (10KΩ-m)	IEEE MGWL 1999
0.05 @ 4GHz	-	Au (5μm)	Pyrex	Exp. data
0.03 @ 4GHz	**Thick oxide (25μm)**	**Cu (10μm)**	**Silicon (8Ω-cm)**	**This work**

Table 1. The insertion loss comparisons of coplanar transmission lines obtained from this work and other research results.

Manufacturing process

To achieve low cost and high performance manufacturing process, we developed Cu-BCB passive process. Cu metal is one of the optimal choice for low conductive metal loss and high-speed operation. We used 10μm thickness Cu process for spiral inductor fabrication and interconnection. For resistors, 20ohm sheet resistance NiCr was used. SiN_x dielectric material is employed as interlayer insulator of MIM(Metal-Insulator-Metal) capacitors. Total three metal layers were used, and one was for NiCr metal contact, bottom metal of MIM capacitor and interconnection between inner part and outer part of spiral inductor, another was for top metal of MIM capacitor and some interconnection, the last was for spiral inductor patterning and element interconnection.

Photosensitive BCB material was used as interlayer between Cu metals in this work. Photo-BCB had been originally developed for use in microelectronics applications, including Multi Chip Module(MCM) and flat panel display. Because the photo-BCB has many attractive properties such as processing compatibility with existing IC manufacturing techniques, low moisture uptake, low cure temperature, rapid thermal curing, high planarization level, low dielectric constant and so on, it was adopted in our process. The BCB

layer of 4.5μm was used for interlayer of metal layers and the BCB layer of 5μm was used for final passivation.

The process flow is as follows. In the first place, Si wafer with thick oxide(25μm) is prepared. And then the SiN_x layer of 1000Å is deposited on whole front side of the wafer to stabilize the microstructure. NiCr is deposited and patterned by lift-off process. Ti/Cu metal evaporation of 5000Å is followed by 1000Å SiN_x dielectric material deposition. Etching process forms the dielectric via and dummy Ti/Cu metal is evaporated to define the top area of MIM capacitor. BCB layer is coated on wafer and BCB via process is performed. Then 10μm Cu plating process and BCB passivation process is performed. Pads are finally opened by BCB etching process. Depending on the applications, final Ni/Au treatment can be done.

Figure 3 shows schematic cross sectional view of passive structures by this process. The developed Cu-BCB process is low cost manufacturing process, compared to Au process typically used in III-V compound industry and is high performance process due to high conductivity of Cu and low dielectric loss of BCB for RF applications, compared to Al process widely used in Si based semiconductor industry. Therefore this is very optimal process for high quality RF passive integration.

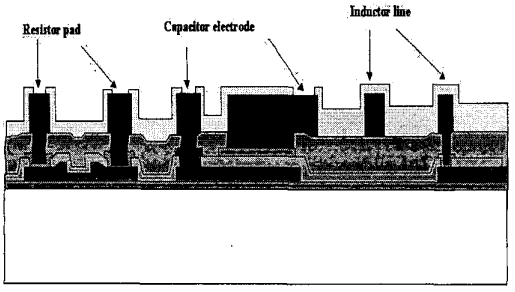


Figure 3. Cross sectional view of passive process on thick oxide substrate

High Q inductors on Si substrate

We resolved one of the major technological challenges in fabricating RF integrated circuit on Si substrate, on-chip inductor implementation, by using low cost porous silicon process and advanced oxidized process to make very thick SiO_2 layer. As mentioned in previous section, to improve inductor performance, BCB interlayer technology and Cu plating technology were used together with our developed thick oxide substrate technology. The on-chip inductors were fabricated with Cu thickness of 10μm on 25μm thick oxide 6" silicon wafer.

Small size spiral inductor of 1.3nH with 10μm line and spacing showed maximum quality factor of ~120 at 6GHz. The fabricated on-chip inductors showed the maximum quality factor range of 30~120, depending on geometrical factors and inductance values of 0.6~35nH. Especially the inductors showed high quality factors in broadband frequency range. For example, the quality factor of 1.3nH Cu spiral inductor was more than 40 up to 12GHz and maximum quality factor was about 120 at 6GHz. The two-port quality factor of the fabricated inductor extracted from the measured data are shown in figure 4.

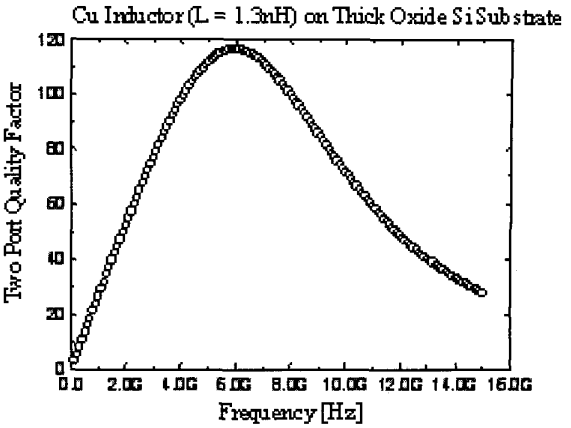


Figure 4. The two-port quality factor extracted from the measured results of 1.3nH Cu inductor

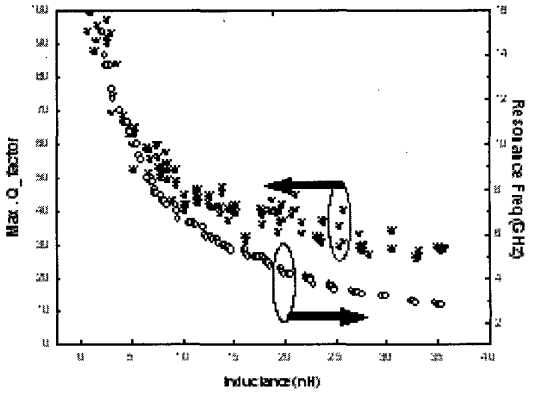


Figure 5. Maximum quality factor and resonance frequency distribution with inductance values of 10μm Cu inductors

These thick oxide substrate technology and high Q inductor technology have the potential not only to push the RF operating window for Si MMICs well into the 10GHz range but also to broaden the area of integrated passive devices, which has been limited to low frequency region of several hundred MHz, up to 10GHz or above

Figure 5 shows the maximum quality factors and resonance frequency distribution with inductance values. In case of inductance values less than 10nH that are commonly used in RFIC, the maximum quality factors have the values more than 50. As shown in figure, the different maximum quality factors and different frequency characteristics are obtained from different geometries, although they have very similar inductance values. Therefore, the circuit designers should choose proper inductors for their specific applications.

RF Integrated Passive Devices

MIM capacitors and NiCr thin film resistors for RF applications can be also integrated on thick oxide substrate, because of its extremely flat surface. These thick oxide

substrate technology and RF passive integration technology of MIM capacitors, resistors, high Q inductors enable to push the RF capability of Si MMICs well into 10GHz range, offering real competition in a regime that they consider the exclusive domain of GaAs and InP. Utilizing high quality passive devices, we fabricated several kinds of integrated passive devices such as low pass filter, power combiner, balun and so on.

Figure 6 shows the fabricated 900MHz lumped low pass filter as an example. Low pass filter layout was configured for wafer level packaging (solder ball bumping) and its size was 0.9mm×0.9mm. Figure 7 shows RF performances of low pass filter that was fabricated on thick oxide wafer using 10μm Cu plating process. At 900MHz, the insertion loss of the filter was about 0.45dB and attenuations in second and third harmonic frequency were less than 25dB, respectively.

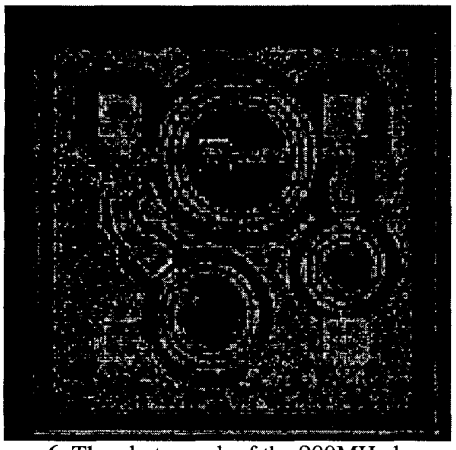


Figure 6. The photograph of the 900MHz low pass filter

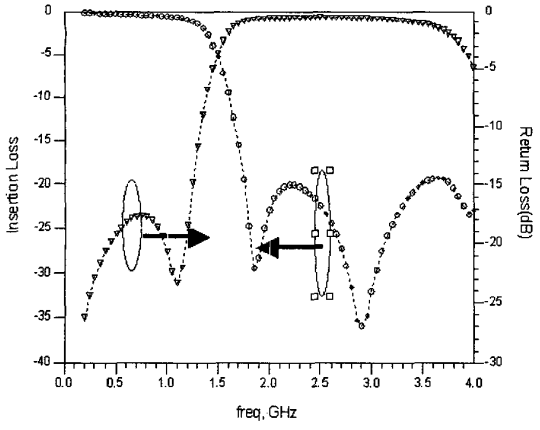


Figure 7. RF performances of 900MHz LC-type lumped low pass filter fabricated on thick oxide wafer

As widely known, it will be actively utilized for small-size front-end module. Cu-based low pass filter has much superior current handling capability to Au-based filter and Al-based filter widely used in Si MMIC industry or GaAs MMIC industry.

In case of 1800MHz power combiner, the chip size is 1.4mm×0.9mm. Figure 8 shows the fabricated 1800MHz power divider. As shown in figure 9, the measured insertion loss is about 0.5dB, the return loss is less than –25dB, and port isolation is greater than 20dB.

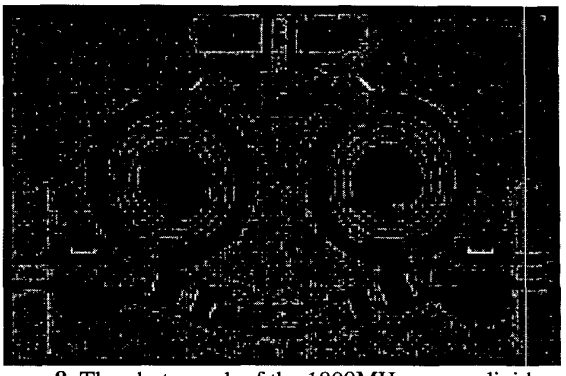


Figure 8. The photograph of the 1800MHz power divider

In case of 1700MHz LC-type lumped balun, the insertion loss was about 0.6dB and amplitude and phase imbalance was less than 0.1dB and 2°, respectively. Four fixed attenuators were implemented on the size of 2mm×2mm for wafer level packaging using solder ball bumping. Π-type circuit topology was applied and attenuation level was constant up to 3.5GHz. All the VSWR's(Voltage Standing Wave Ratio) were less than 1.3, although they were depending on the attenuation levels.

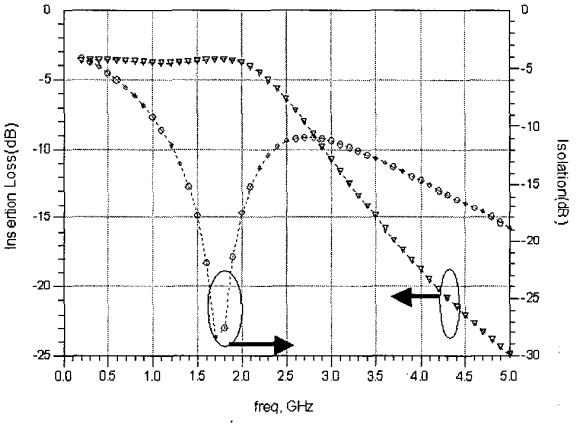


Figure 9. RF performances of 1800MHz LC-type lumped power divider fabricated on thick oxide wafer

Although the fabricated integrated passive devices were not fully optimized in terms of circuit topology and remained to be improved, low cost and small-form-factor microwave passive devices that showing good performances in microwave region were successfully fabricated and evaluated on 6" silicon wafer with our new technology. These integrated passive devices will be the optimal solution for hand-held module and system where the size or volumetric efficiency is a critical buying criterion.

Conclusions

The requirements of cost and size reduction push all the companies in the supply chain to find new solution out for their product competence. Up to now, there have been many

researches on RF passive integration on Si wafer for low cost and mass-producible process. However, they have not provided satisfactory solutions and the results were not be utilized in commercial industry. Based on this industry demand, we have developed low cost manufacturing technology for RF substrate and high performance passive process technology for RF integrated passive devices by forming thick oxide on Si wafer and using Cu metal and BCB interlayer material. The fabricated substrate of 25μm oxide thickness showed good insertion loss of 0.03dB/mm at 4GHz, in case of coplanar transmission line with W=50μm and G=20μm, which included the conductive metal loss. Especially the transmission line showed high performance up to more than 10GHz. The insertion loss was below 0.1dB/mm up to 15GHz. It was much superior to that of expensive HRS(High Resistivity Silicon, 7Kohm-cm) substrate. Based on these well-developed processes, we achieved ultra high Q inductor on Si wafer, which showed the maximum Q factor of 120. To the knowledge of the authors, it is the highest value on Si substrate in the world. The fabricated on-chip inductors showed the maximum quality factor range of 30~120, depending on geometrical factors and inductance values of 0.6~35nH. Especially the inductors showed high quality factors in broadband frequency range. For example, the quality factor of 1.3nH Cu spiral inductor is more than 40 up to 12GHz and maximum quality factor is about 120 at 6GHz. We fabricated RF integrated passive devices with small form factor. They showed good RF performances in spite of small chip size.

These thick oxide technology and high quality RF passive integration technology of MIM capacitors, resistors and high Q inductors have the potential to push the RF operating windows for Si MMICs well into the 10GHz, offering real and keen competition in a regime that they consider the exclusive domain of GaAs and InP. And also these will broaden the area of integrated passive devices, which has been limited to lower frequency region of several hundred MHz, up to more than 10GHz. Finally the developed technologies in this paper will be widely utilized in hand-held module and system where the size or volumetric efficiency is a critical buying criterion.

Reference

[1] Robert H. Cavely, Scott Smith, Jiangang Hu, and Robert Nochols, "CMOS RF Circuits for Integrated Wireless Systems," *in MTT-S International Microwave Sym. Digest*, pp. 1851-1854, 1988

[2] Abidi A, "CMOS-only RF and Baseband Circuits for a Monolithic 900MHz Wireless Transceivers," *in Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology*, pp. 35-42, 1996

[3] Takahashi C., Fujimoto R., Arai S., Itakura T., Ueno T., Tsurumi H., Tanimoto H., Watanabe S., and Hirakawa K., " A 1.9GHz Si Direct Conversion Receiver IC for QPSK Modulation Systems," *in IEEE ISSCC Dig. Tech Papers*, 138-139, 1995

[4] Khabbaz B., Douglas A., DeAngelis J., Hongsmatip L., Pelliccia V., Fahey W., and Dawe G., " A High Performance 2.4GHz Transceiver Chip-set for High Volume Commercial Applications," *in IEEE Microwave and Millimeter-Wave Monolithic Circuits Symp.*, pp. 11-14, 1994

[5] Tanaka S., Hase E., Nakajima A, Sugano K., Fujioka T., Imakado Y., Fujiwara K., Okamoto T., Shigeno Y., Sato K., Arai I., Yamane M., Kusano C., Sakamoto K., Nakagawa J., and Koya M., " A 3V MMIC Chip Set for 1.9GHz Mobile Communication Systems," *in IEEE ISSCC Dig. Tech Papers*, pp. 144-145, Feb. 1995

[6] Kobayashi K.W., Nishimoto M., Tran L.T., Huei Wang, Cowles J.C., Block T.R., Elliott J.H., Allen B.R., Oki A.K., and Streit D.C., "A 44GHz High IP3 InP Amplifier with Practical Current Reuse Biasing, IEEE Trans. Microwave Theory Tech., vol. 46, no. 12, pp. 2541-2552, 1998

[7] A.C. Reyes, " Silicon as Microwave Substrate," *in IEDM Tech. Digest*, pp. 1759-1762, 1995

[8] H. Sakai, " A New Millimeter-Wave IP-Chip on Silicon Substrate," *in Asia Pacific Microwave Conference*, pp. 291-294, 1994

[9] B.K. Kim, B.K. Ko, and K. Lee, " Monolithic Planar Inductor and Waveguide Substrate on Silicon with Performance Comparable to Those in GaAs MMIC," *in IEDM Tech. Digest*, pp. 717-720, 1995

[10] Choong-Mo Nam and Young-Se Kwon, " High Performance Planar Inductor on Oxidized Porous Silicon(OPS) Substrate," IEEE Microwave Guided Wave Letters, vol. 7, no. 8, pp. 236-238, 1997

[11] Han-Su Kim, Dawei Zheng, A. J. Becker and Ya-Hong Xie, " Spiral Inductors on Si p/p^+ Substrate with Resonant Frequency of 20GHz," IEEE Electron Device Letters, vol. 22, no. 6, pp. 275-277, 2001