300 W GaN Power Amplifier for LTE Applications

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***Abstract*—This paper presents a 300 W GaN power amplifier operating in the LTE band 7 (2.62~2.69 GHz). From the loadpull simulation, optimum impedances of the GaN HEMT at the fundamental frequency and the second harmonic frequency are extracted for a maximum output power. The matching circuits that give the nearly optimum second harmonic impedances are implemented on a titanate substrate with a high dielectric constant and are integrated with a bare GaN transistor in a ceramic package. The fabricated power amplifier shows a saturated output power of 258~324 W and a drain efficiency of 67~73 % under the pulsed condition of 1 msec period and 10 % duty cycle. It also has an output power of 80~85 W and a drain efficiency of 42~49 % at ACLR of 30 dBc with the LTE input signal.**

Keywords—GaN; power amplifier; internally matched FET; second harmonic tuning; LTE

I. INTRODUCTION

Base stations and repeaters for cellular communications require high linearity, high efficiency and high power amplifiers for a wide cell coverage. A GaN high electron mobility transistor (HEMT) has a superior power density, compared with a Si laterally diffused metal oxide semiconductor (LDMOS) transistor or GaAs HEMT, and its market share rapidly increases as the GaN process becomes stable and reliable. The GaN HEMT tends to increasingly replace the conventional counterparts, especially in the base stations of LTE cellular communications [1].

Since a power amplifier in a transmitter consumes the most power in an RF system and suffers from thermal dissipation problems affecting the system reliability, a drain efficiency (or power-added efficiency) is one of the most important interests. To achieve a high efficiency, Class E and Class F switching power amplifiers are typically preferred. The former has a simple configuration, but its output performance is sensitive to an inherent parasitic capacitance of the transistor in a GHz frequency range, while the latter needs impedance tuning at multiple harmonics in addition to the fundamental impedance matching for obtaining enough efficiency, and the impedance tuning complicates output matching circuits [2]-[4].

In this paper, we present an internally matched 300 W GaN power amplifier for LTE band 7 base stations that consists of a bare die transistor, CGHV40320D of the Cree Inc. and thin film input/output matching circuits in a ceramic package. The input matching circuit simultaneously provides the optimum fundamental impedance and the optimum second harmonic impedance for the high efficiency by using open stubs. The output matching is performed in a typical way in which the matching circuit is first designed for the optimum load impedance at the fundamental frequency and then tuned for the second harmonic impedance range where no significant output power and efficiency degradations are observed.

II. OPTIMUM IMPEDANCE EXTRACTION FROM GAN HEMT

Figure 1 shows a GaN bare die HEMT of the Cree Inc. that has a size of 6.1×1.1 mm^2 and is typically used up to 4 GHz [5]. The transistor has a drain breakdown voltage of 150 V, and shows an estimated maximum output power of 347 W, a maximum drain efficiency of 69.7 % and a maximum stable gain of about 23 dB at 2.7 GHz at the bias condition of V_{ds}=50 V and I_{ds}=500 mA.

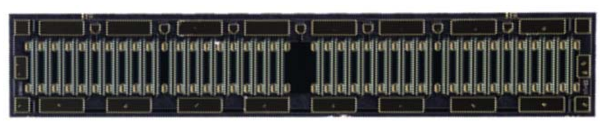
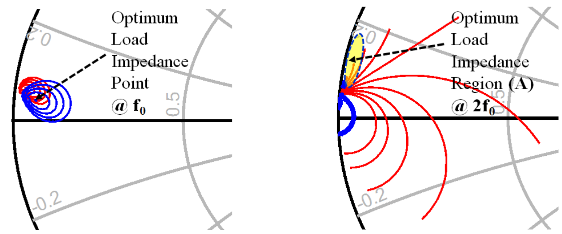


Fig. 1. 300 W bare die transistor of the Cree Inc. (CGHV40320D)

From the loadpull simulation using a nonlinear transistor model, impedance contours of the output power and drain efficiency at the fundamental and second harmonic frequencies are obtained and illustrated in Fig. 2. Figure 2(a) shows the load impedance contours at 2.65 GHz for the output power and drain efficiency, respectively, and has the maximum output power of 302 W and the maximum drain efficiency of 70 % at their respective optimum impedance points, with the harmonic impedances not optimized. With the fundamental source and load impedances at the optimal points, figure 2(b) shows the effect of the second harmonic load impedance on the output power and drain efficiency. With the proper choice of the second harmonic impedance



(a) power/drain efficiency contours at the fundamental frequency (2.65 GHz)

(b) power/ drain efficiency contours at the 2nd harmonic frequency

Fig. 2. The output power and drain efficiency contours at the fundamental and second harmonic frequencies from the loadpull simulations (blue: P_{out}, red: drain efficiency)

(region A in Fig. 2(b)), the output power and drain efficiency can be enhanced to 357 W and 77 %. According to the harmonic loadpull simulation, the third harmonic load impedance affects little on the output performance. Table I summarizes the optimum source and load impedances of the GaN HEMT at the fundamental and second harmonic frequencies that are extracted from the sourcepull and loadpull simulations.

TABLE I. Optimum source and load impedances of the transistor at the fundamental (center frequency of the bandwidth) and second harmonic frequencies

Impedance / Frequency	f_o=2.65 GHz, V_{ds}=50 V, I_{ds}=500 mA	
	optimum source impedance [Ω]	*optimum load impedance [Ω]*
Fundamental	0.550 + j 0.623	2.141 + j 2.532
2nd harmonic	0.180 + j 0.640	0.182 + j 3.690

III. Power Amplifier Design and Fabrication

The power amplifier is biased at the class-AB condition of V_{ds}=50 V and I_{ds}=500 mA, and the transistor is integrated together with thin film pre-matching circuits in a ceramic package. The matching circuits simultaneously achieve the required fundamental and second harmonic impedance conditions and are fabricated on the titanate substrate with high relative dielectric constant ε_r of 40. Slight impedance mismatches on the input and output ports are tuned using microstrip lines on a Tanonic RF35TC substrate.

Figure 3 shows a schematic circuit of the pre-matched power amplifier with the second harmonic impedance tuning circuits on the high ε_r substrate in a ceramic package. The transistor is divided into 8 unit cells; each cell is pre-matched with the second harmonic open stubs on the input and the second harmonic tuning elements of stepped impedance microstrip lines on the output. The open stub provides a high shunt impedance at the fundamental frequency and a nearly short impedance at the second harmonic frequency. The

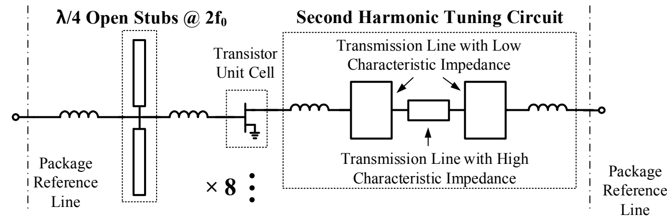


Fig. 3. Schematic circuit of the pre-matched power amplifier with the second harmonic impedance tuning network in a package

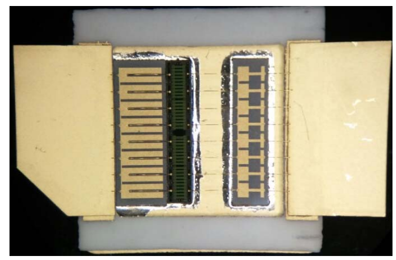


Fig. 4. Photograph of the fabricated GaN power amplifier with the pre-matching circuits and the second harmonic tuning circuits in the package

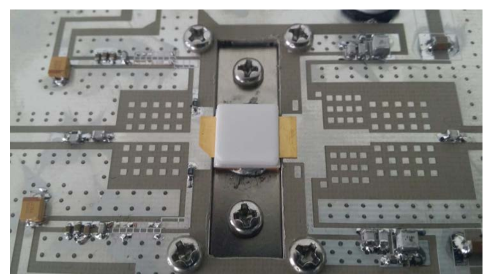


Fig. 5. Photograph of the fabricated power amplifier with external PCB matching circuits for measurement

output pre-matching circuit moves the transistor's output impedance to the impedance point that makes the impedance matching easy and achieves the second harmonic impedance matching. All the bonding wires are electromagnetically simulated to fully consider the wire bonding looping. The pre-matched power amplifier in the package has the input impedance of 18.35 – j 2.26 Ω and the output impedance of 3.539 – j 4.541 Ω at the package reference plane.

Figure 4 shows the photograph of the fabricated GaN power amplifier with the pre-matching circuits and the second harmonic tuning circuits integrated in the package. The bare die is eutectic-bonded to the CPC package bottom, and 1 mil wedge bonding is used for an electrical connection. Figure 5 shows the fabricated power amplifier with external matching circuits that are implemented on the RF35TC substrate. DC bias circuits and quarter-wavelength impedance transformers are fabricated on the substrate, together with a RC parallel stabilizing circuit.

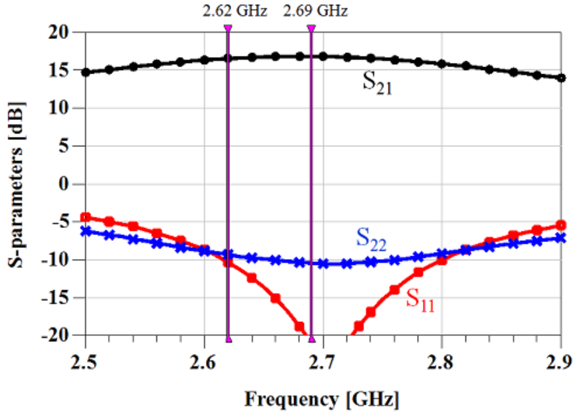


Fig. 6. Measured S-parameter results

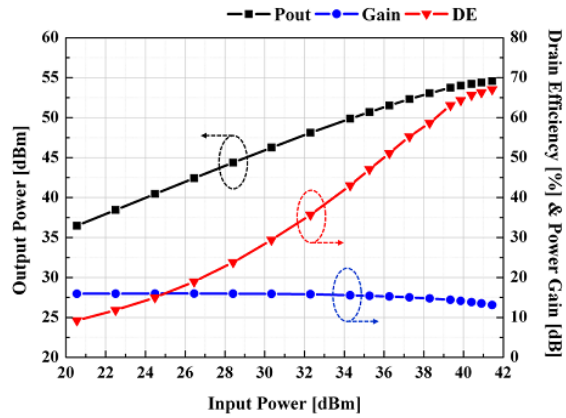


Fig. 7. Measured output power, drain efficiency and power gain with the input power at 2.65 GHz under the pulsed condition (T=1 msec, D=10 %)

IV. MEASUREMENT RESULTS

Figure 6 shows measured S-parameter results at V_{ds}=50 V and I_{ds}=500 mA. The fabricated power amplifier has a linear gain of 16.6~17.3 dB and a return loss of better than 10 dB in 2.62~2.69 GHz. Figure 7 shows measured power performance with the input power at 2.65 GHz in a pulsed mode of 1 msec period and 10 % duty cycle. The power amplifier shows an output power of 258~324 W and a drain efficiency of 67~73 % with an associated power gain of 11.5~14.0 dB in 2.62-2.69 GHz. Table II summarizes the power performance measured at three frequencies of 2.62 GHz, 2.65 GHz and 2.69 GHz corresponding to LTE band 7.

The fabricated power amplifier is used for the base station of LTE applications, and therefore should meet the adjacent channel leakage ratio (ACLR) specification. It shows an output power of 80~85 W and a drain efficiency of 42~49 % with the ACLR of 30 dBc, as shown in Fig. 8.

TABLE II. MEASURED POWER PERFORMANCE IN THE LTE BAND 7

Frequency	V_{ds}=50 V, I_{ds}=500 mA (DC bias point) 1 msec pulse width and 10 % duty cycle		
	Output Power	***Power Gain***	***Drain Efficiency***
2.62 GHz	54.1 dBm	11.5 dB	71.1 %
2.65 GHz	54.6 dBm	13.1 dB	67.1 %
2.69 GHz	55.1 dBm	14.0 dB	72.7 %

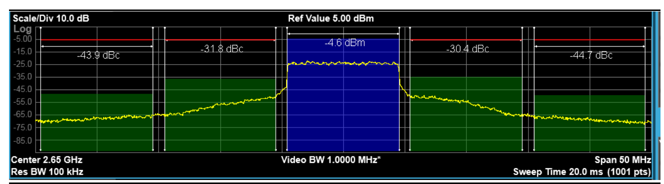


Fig. 8. Output spectrum with the LTE input signal under the condition of the 30 dBc ACLR

V. CONCLUSION

The 300 W internally matched power amplifier is developed for the LTE base stations using the GaN bare die transistor and the thin-film matching circuit on the titanate substrate in the ceramic package. The power amplifier obtains a high drain efficiency of 67~73 % by using the second harmonic impedance tuning circuit while providing the saturated output power of 258~324 W in 2.62~2.69 GHz. The developed power amplifier can be effectively used in the LTE communication systems.

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