PASSIVE MINIATURIZATION: SI INTEGRATED PASSIVE DEVICES FOR RF AND MICROWAVE APPLICATIONS

With well-developed, low cost RF passive manufacturing technology (thick oxide Si substrate and copper/benzocyclobutene (Cu/BCB) multi-layer passive process technologies), various kinds of high performance RF integrated passive devices (IPD) have been fabricated on a 6" Si wafer for RF and microwave applications, and have achieved dramatic cost and size reductions. The fabricated devices are a low pass/high pass antenna diplexer, a low pass filter with harmonic resonance, a bandpass type diplexer for a VCO loop and a 2.4 GHz wireless LAN balun. To the authors' knowledge, they offer the smallest size and highest performance for devices of this type built on silicon. The size of the wafer-level, packaged, RF IPD is 1 to 1.5 mm^2. This RF passive integration technique will permit the 40 percent functional size reduction for handheld phones and wireless terminals that has been pursued until now.

When considering mobile electronic products, smaller is usually better. Most portable devices often have particularly stringent miniaturization requirements in order to meet market place expectations. The average passive device count in cellular phones has not dramatically dropped in recent years[1] and current handset designs are far from eliminating passive components. The size improvements, to date, have come from both smaller passive components and more efficient packaging of the components on the boards. The market demands, such as ultra-miniaturization and pricing pressure, make the integration of passive components on wafer to be the solution for the next generation of mobile terminals. There has been considerable research focused on low temperature and low cost co-fired ceramic (LTCC) technology,[2] but the research on thin film multi-chip module with deposited substrate (MCM-D) technology is not active. It is mainly focused on glass carrier substrates,[3] not on Si substrates because of many limiting factors such as substrate conduction.

A thick oxide technology has been developed to transform the Si wafer in a new RF

DONG-WOOK KIM, IN-HO JEONG AND JONG-SOO LEE
Telephus Inc.
Taejeon, South Korea

substrate and synergistically combine it with a high quality passive Cu/BCB process.[4,5] Device examples and measured results for various RF IPDs are provided to demonstrate their superior performance and attractive size reduction. To reduce the size of the passive component to the maximum, PbSn eutectic solder balls are used to attach them directly on the board.

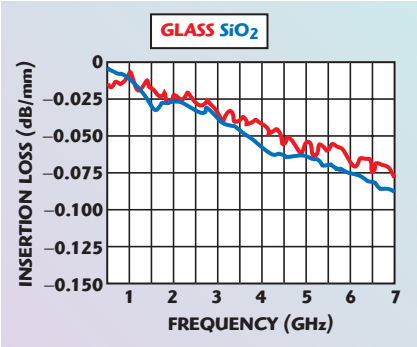
PASSIVE INTEGRATION ON SI SUBSTRATE

Silicon is the most stable and reliable semiconductor and has been used in many electronic applications. Unlike other semi-insulating substrates, silicon has had to rely on the properties of silicon dioxide for isolation. But a thin silicon dioxide layer cannot effectively isolate passive devices on Si substrates because of capacitive effects. The signal loss is also high because of the finite conductivity of the silicon substrate. These effects make it difficult to use Si technology for RF and microwave applications. In addition to the substrate loss, the conductor loss in the metals, due to the low conductivity of materials such as aluminum, limits the application of silicon to less than a few hundreds of megahertz.

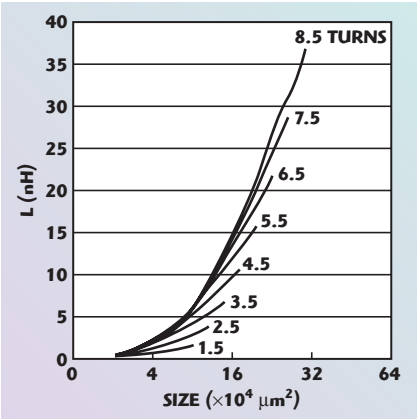
A thick silicon dioxide layer of 25 µm on Si reduces the transmission losses by confining most of the electromagnetic field in the low loss dielectric layer beneath the conductors and not in the conducting silicon region. Also, the use of an 11 µm thick Cu metal layer and low dielectric constant BCB material makes it possible to implement low loss transmission lines over a broad frequency range. For example, a 50 Ω coplanar transmission line of 50 µm width and 15 µm gap on Si showed a total insertion loss of only 0.04 to 0.07 dB/mm at 5 GHz. This RF loss is very comparable to that of a high quality glass substrate in the low GHz region, though the latter shows slightly higher performance in the frequency region above 10 GHz. However, the glass substrate is very fragile and can break easily during the process. ***Figure 1*** shows a comparison of the insertion losses of coplanar waveguide (CPW) lines built on a thick oxide Si substrate and a high quality glass substrate. The results show that the specialized Si substrate and Cu process can be the optimal choice for low cost and high performance RF passive integration. For small-size passive devices, the area occupied by an inductor should be reduced, while maintaining satisfactory RF performance. To achieve this goal, a line width of 10 µm and a line spacing of 10 µm are mostly used for functional passive devices on Si. ***Figure 2*** shows the inductance value as a function of the number of turns and inductor size. Most of the planar spiral inductors occupy less than 0.5 × 0.5 mm area and are mostly concentrated in the 0.09 to 0.16 mm^2 region. They are much smaller than any other inductors implemented on PCB, LTCC or glass substrates.

SMALL-SIZE AND HIGH POWER RF INTEGRATED PASSIVE DEVICES

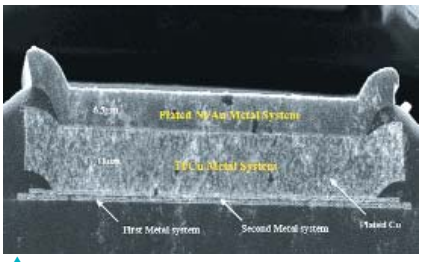
The on-chip inductor, a major technological challenge, is fabricated on a thick oxide Si substrate using a Cu metal system with 11 µm plated metal thickness and BCB interlayer material. The fabricated inductors have a spacing of 10 µm between turns and several different metal widths (10, 20, 30, 40, 50 µm) and show the maximum quality factor Q for the range of 40 to 60 µm, depending on the geometrical parameters and for inductances from 0.3 to 35.0 nH. ***Figure 3*** shows a cross-sectional view of the bonding pad structure composed of Ti/Cu – Ni/Au and BCB passivation. The Ni (6 µm) and Au (0.5 µm) layers are electroplated and used for the bonding of Au wire. They are not needed when the chip is bonded with solder balls during packaging. The spiral inductor with thick Cu metal has much more DC current and RF power capabilities than conventional Al- or Au-based inductors, even though the underlying interconnection between inner and outer sides of the inductor is relatively thin. The DC current test results for a spiral inductor with a 10 µm line width and line spacing is shown in ***Figure 4***. Every current step was sustained for 15 minutes and the current was increased to 640 mA. According to the data, some deviation was observed around 550 mA and the underlying metal started to burn at more than 600 mA. No physical or performance change was noticed after the inductor was submitted to a DC current of 500 mA for 168 hours. RF components for wireless applications are typically required to have an RF CW power handling capability of 3 W. The input and output matching circuits fabricated using the Cu process endured 5 W of RF power for 168 hours without change,



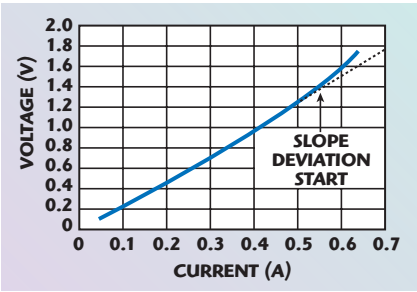
▲ *Fig. 1 Insertion loss of coplanar transmission lines on 25 µm thick oxide Si substrate and high quality glass substrate.*



▲ *Fig. 2 Inductance as a function of size and number of turns.*



▲ *Fig. 3 Cross-sectional view of a bonding pad.*



▲ *Fig. 4 DC current rating test of the spiral inductor.*

which means the developed small-size Si RF IPD can be considered to have greater power handling capability than required by commercial specifications for handheld terminals.

In the following paragraphs, high quality Si integrated passive devices with high volumetric efficiency will be introduced and their measured performance provided. All the passive devices are wafer-level bonded to the boards, using eutectic solder balls for direct attachment, or are finished with Ni/Au plated pads for wire bond attachment on multi-chip modules. Typically, wire bondable passive devices are 20 to 30 percent smaller than solder ball bonded devices.

LUMPED L-C TYPE LOW PASS FILTER FOR PAM OR FEM APPLICATIONS

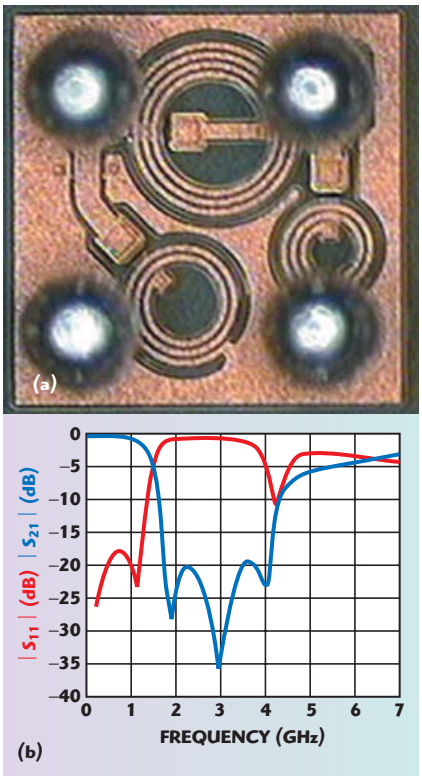
In modern communications systems, low pass filters are used to pass the wanted signal and eliminate or attenuate harmonics, mainly at the output stage of the power amplifier. With conventional low pass filter circuits, it is not easy to meet the insertion loss in the pass-band and the attenuation levels at the second- and third-harmonic frequencies required by strict commercial specifications. While achieving low insertion losses, enough harmonic attenuation was obtained by modifying the Chebyshev filter and the elliptic filter topologies to resonate at harmonic frequencies. ***Figure 5*** shows a 900 MHz low pass filter for GSM applications and its measured results. As shown, the insertion loss is typically 0.45 dB and, in the case of a wafer-level packaged device, the second- and third-harmonic attenuation levels are greater than 25 dBc. The size of the filter is 1.0 mm^2 and it can be directly attached on the PC board by a conventional solder-reflow process. This ultra-miniaturization is sure to be an important step for a 40 percent size reduction in the functional integration of mobile phones.

LOW PASS/HIGH PASS LUMPED L-C DIPLEXER FOR ASM OR FEM APPLICATIONS

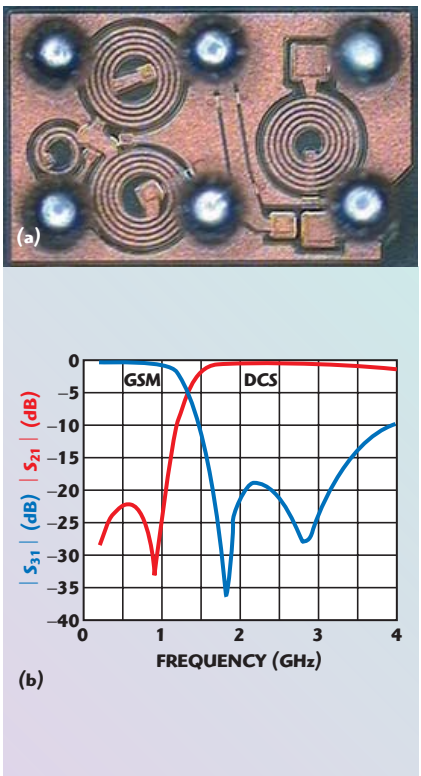
The diplexer handles two different carrier frequencies on the same signal path. It consists of a combination of low pass and high pass filters or two bandpass filters. The bandpass diplexer shows good attenuation characteristics but is very lossy, so it cannot be used in the front end of a mobile phone that does not allow for any excessive loss. ***Figure 6*** shows a fabricated GSM/DCS diplexer and its measured performance. To achieve the high band-rejection level and harmonic attenuation level, four inductors are used to obtain series and parallel resonances. The insertion losses of the wafer-level packaged diplexer are 0.45 dB at 900 MHz and 0.6 dB at 1800 MHz. The band-rejection levels are greater than 25 dBc at 900 MHz and 30 dBc at 1800 MHz. The third-harmonic attenuation is also more than 25 dBc. The size of the wafer diplexer is 1.5 mm^2, corresponding to a 60 percent reduction over a conventional device size.

BANDPASS TYPE LUMPED L-C DIPLEXER FOR VCO LOOP APPLICATIONS

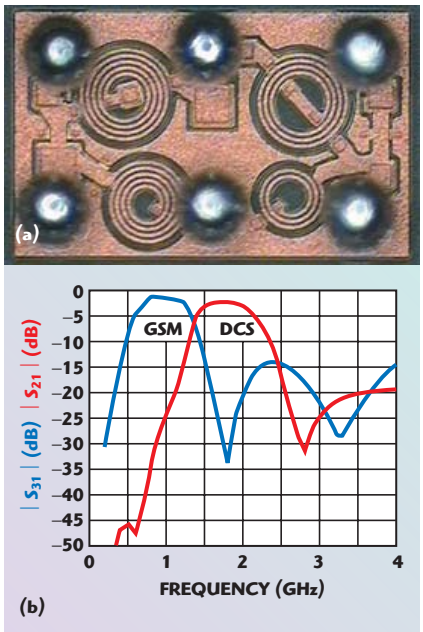
This bandpass type diplexer, providing bandpass filtering and impedance matching, is designed to operate as an EGSM/PCS/DCS transmitter VCO sampling diplexer. It can be used for a two-port, low power transmitter VCO feedback to the synthesizer in GSM handsets. The device circuit consists of bandpass filter channels where suppression of second- and third-harmonic signals is required. Two parallel resonators are used in series connection and shunt connection in each channel. ***Figure 7*** shows the fabricated chip and its test results. The nominal values of the pass-band insertion loss are 1.2 dB at 880 to 915 MHz



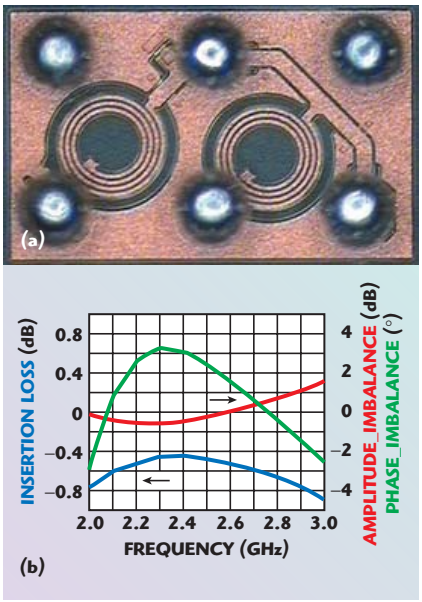
▲ *Fig. 5 Wafer-level packaged low pass filter (a) and its measured results (b).*



▲ *Fig. 6 GSM/DCS diplexer (a) and its measured results (b).*



▲ *Fig. 7 Bandpass type EGSM/PCS/DCS diplexer (a) and its measured results (b).*



▲ *Fig. 8 Balun for 2.4 GHz wireless LAN applications (a) and its measured results (b).*

and 2.2 dB at 1710 to 1910 MHz. The attenuation levels of the stop-band are more than 30 dBc at 1800 MHz and 20 dBc at 3600 MHz. The return loss is greater than 15 dB. The packaged device size is 1.5 mm^2.

LUMPED L-C BALUN FOR WIRELESS LAN APPLICATIONS

A balun converts a balanced signal to an unbalanced one or vice-versa. The photograph and the measured performance of a fabricated 2.4 GHz balun are shown in ***Figure 8***. The insertion loss of 0.5 dB is obtained from back-to-back measurement of the baluns. The phase imbalance is measured to be less than 3.5° and the amplitude imbalance is less than 0.5 dB. These results are superior to those from their ceramic counterparts, which show typical phase imbalance of 10° and amplitude imbalance of 2.0 dB maximum. The smaller size, 1.5 mm^2, corresponding to a reduction of 60 percent over the conventional device, is another advantage.

DISCUSSION

To make RF integrated passive devices small and inexpensive, no packaging was used, except eutectic solder balls for wafer-level bonding. The device with eutectic solder balls can be directly attached to the board, using conventional surface-mount technology (SMT) techniques and a solder-reflow process. Solder balls with a diameter of 130 or 300 µm can be used, depending on the requirements. The former is obtained during the plating process and the latter is typically achieved with the ball placement process. The fabricated passive devices can be RF-tested using a membrane probe card. According to the experiments performed, the solder balls are not damaged too much and the RF measurement results are accurate and reproducible if the probe contact is kept to less than 20 times for the same device. When less than 20 contacts have been made, the measurement error is less than 0.05 dB and the standard deviation is 0.016 dB.

CONCLUSION

Small-size RF integrated passive devices are fabricated on 25 µm thick oxide Si substrates, using a thick Cu and low dielectric constant BCB interlayer processes. The devices show high RF power handling capability (more than 3 W) and low loss. Solder bumps for passive device bonding are used and to the authors' knowledge, the fabricated wafer-level packaging circuits shown here are the smallest ever reported, compared to conventional ceramic passive devices. The low pass filter shows an insertion loss of 0.45 dB and the harmonic attenuation level is greater than 25 dBc. The packaged device size is 1.0 mm^2. The antenna diplexer for GSM/DCS applications shows insertion losses of 0.45 and 0.60 dB at 900 MHz and 1800 MHz, respectively. The band-rejection levels are more than 25 dBc at 900 MHz and 30 dBc at 1800 MHz. The insertion losses of the diplexer for VCO applications are 1.2 dB at 900 MHz and 2.2 dB at 1800 MHz, in spite of the band-pass topology. A balun is also fabricated for 2.4 GHz wireless LAN applications and has a loss of 0.5 dB, a phase imbalance less than 3.5° and an amplitude imbalance less than 0.5 dB. The size of the above three passive device circuits is 1.5 mm^2 and shows a dramatic reduction compared to conventional approaches. The "cheap and small" passive devices are achieved by using passive integration technology on Si substrates and wafer-level solder bump bonding, while maintaining their high power handling capability and RF performance. This RF passive integration on Si will provide a step forward for the next generation of mobile technology and will be cost-effective. It is an optimal solution for handheld wireless applications that require stringent cost and size reductions. ■

References

1. D. Carey, "Miniaturization in Electronics: The Passive-aggressive View," Passive Component Industry, September/October 2001, pp. 28–30.
2. J. Muller, "High Quality RF Inductors in LTCC," Proceedings of the ISHN International Symposium on Microelectronics, Minneapolis, MN 1996.
3. W. de Raedt, E. Beyne and R. Mertens, "Thin Film Embedded Passives for Microwave and Millimeter-wave Applications," 7th Pan Pacific Microelectronic Symposium, Hawaii, 2002, pp. 343–349.
4. D.W. Kim, I.H. Jeong, C.M. Nam, T.O. Kong, H.S. Sung, K.J. Kim, I.D. Yoon, J.S. Lee and Y.S. Kwon, "Ultra High Q Inductor and RF Integrated Passive Devices on Thick Oxide Si Substrate," 7th Pan Pacific Microelectronics Symposium, Hawaii, 2002, pp. 350–355.
5. D.W. Kim, I.H. Jeong, H.S. Sung, J.S. Lee, C.M. Nam and Y.S. Kwon, "High Performance RF Passive Integration on Si Smart Substrate," IEEE International Microwave Symposium, Seattle, WA 2002.

Dong-Wook Kim *received his BS degree in electronics engineering from HanYang University, Seoul, South Korea, in 1990, and his MS and PhD degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Taejeon, South Korea, in 1992 and 1996, respectively. From 1991 to 2000, he worked as a member of the technical staff at the LG Electronics Institute of Technology, Seoul, South Korea, where he was involved in developing microwave and millimeter-wave circuits and modules. Since 2000, he has been a principal engineer and general manager of Telephus Inc., where he is currently leading the product development division to develop Si integrated passive devices and multi-chip modules for microwave and millimeter-wave applications. His areas of interest are low cost passive integration techonology, RF and millimeter-wave integrated circuit design, multi-chip module based on low cost passive integration process and system-in-package. Dr. Kim is a member of both IEEE and IMAPS (International Microelectronics and Packaging Society).*

In-Ho Jeong *received his MSEE and PhD degrees from the Korea Advanced Institute of Science and Technology (KAIST), Taejeon, South Korea, in 1997 and 2001, respectively. He currently works for Telephus Inc. as a senior R&D engineer. His research interests include RF MEMS technology and integrated passive devices for wireless communications.*

Jong-Soo Lee *received his BSEE, MSEE and PhD degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST) in 1994, 1996 and 2001, respectively. In 2000, he was a research engineer at the DaimlerChrysler Research Center, Ulm, Germany, working with GaN power amplifiers. He joined Telephus Inc. that same year. His work includes passive device modeling for MCM-D technology, design of passive circuits, and the design of RF modules integrated with passive circuits, SAW-based filters and RFICs. His major interests are in active devices such as Si BJT or BiCMOS and GaAs (InP) MESFET, HEMT or HBT to design RF subsystems or modules such as transceiver modules including diplexers, LNAs, filters and mixers.*