A K-Band CMOS Voltage Controlled Delay Line Based on an Artificial Left-Handed Transmission Line

Choul-Young Kim, *Student Member, IEEE*, Jaemo Yang, *Student Member, IEEE*, Dong-Wook Kim, *Member, IEEE*, and Songcheol Hong, *Member, IEEE*

***Abstract*—A K-band voltage controlled delay line based on a left-handed transmission line (LHTL) with cascaded metal-oxide-semiconductor (MOS) varactors and shunt inductors using CMOS technology is demonstrated for the first time. A variable time delay can be obtained by changing the capacitance of MOS varactors without any power consumption. The figure of merit is 10.9°/dB at 18 GHz. This result is better than other variable LHTL in similar frequency band. A time delay ranging from 56.8 ps to 76.4 ps is achieved at 18 GHz. It allows about 30 times longer time delay than that of a traditional right-handed one with the same length. The chip size, including the pads, is 410 μm × 640 μm.**

***Index Terms*—CMOS delay line, left-handed transmission line (LHTL), variable time-delay line.**

I. Introduction

MICROWAVE delay lines have been widely used in many applications such as radar and phased array systems. Recently, the implementation of a compact module has been the key issue in reducing the cost and size of these applications [1], [2]. There are many kinds of delay lines, such as optical delay lines, magnetostatic wave delay lines, surface acoustic wave delay lines, high-temperature superconducting delay lines, and transmission line delay lines [3]–[6]. The delay lines based on a transmission line have low loss and wide band characteristics; they are also suitable for a single chip, though they also need a larger area than other delay lines. Left-handed transmission lines (LHTLs) are widely used for small microwave passive components [7], [8]. LHTLs can have more time delay than right-handed transmission lines (RHTLs) because in LHTLs the phase constant, β, can be much larger than that of RHTLs [9]. Thus, a compact delay line can be made using an LHTL structure in a microwave integrated circuit and a monolithic microwave integrated circuit. Microstrip LHTLs and delay lines based on microstrip LHTLs were implemented with planar transmission lines periodically loaded with interdigital capacitances and short-stub inductances at 1.5 and 9.5 GHz, respectively [9], [10]. Tunable LHTLs were implemented with various varactors, such as ferroelectric varactors and diode varactors in hybrid circuits, [12]–[17].

For this letter, we use, for the first time, CMOS technology to demonstrate a K-band voltage controlled delay line based on an artificial LHTL with cascaded metal-oxide-semiconductor (MOS) varactors and shunt inductors.

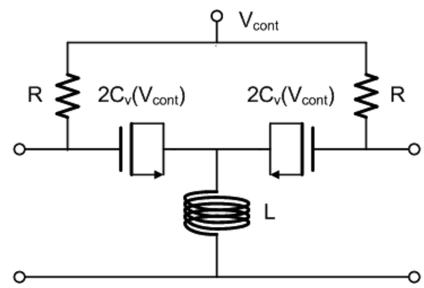

Fig. 1. Unit cell of a voltage controlled delay line based on an artificial LHTL.

II. Circuit Design

The LHTL can be realized artificially in the form of a lumped-elements ladder network. Fig. 1 shows the unit cell of a delay line based on an artificial LHTL. The proposed delay line was fabricated with 0.18 μm CMOS technology, which provides one poly layer for the gate of the MOSFET and six metal layers for interconnection. The total circuit of the delay line based on an LHTL, as shown in Fig. 1, is composed of four sections of a unit cell. The transmission line inductor can be realized by using the top metal as a signal line and the bottom metal as a ground with a thick SiO_2 layer as a substrate. The top metal and the bottom metal are fabricated with Al metals that have a thickness of 2 μm and 0.5 μm, respectively. The metals are separated by an oxide layer approximately 6.5 μm thick. Thus, the loss associated with a silicon substrate can be reduced. The MOS varactors are used for capacitances. An artificial LHTL formed by cascading several unit cells together has a periodic cutoff frequency, ω_B, which is known as the Bragg frequency [11]. The operating frequency must be higher than the Bragg

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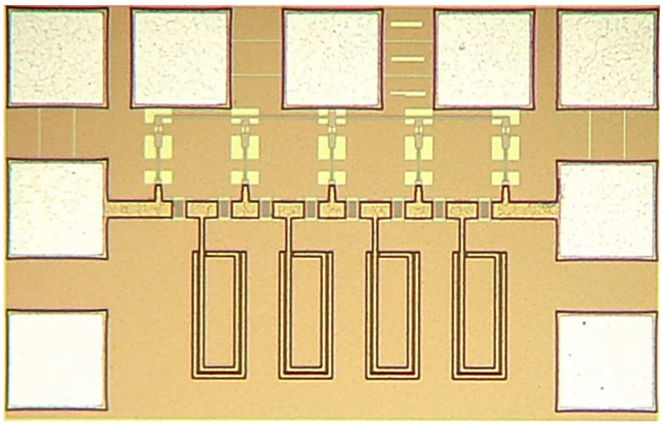

Fig. 2. Chip photograph of the fabricated voltage controlled delay line based on an artificial LHTL.

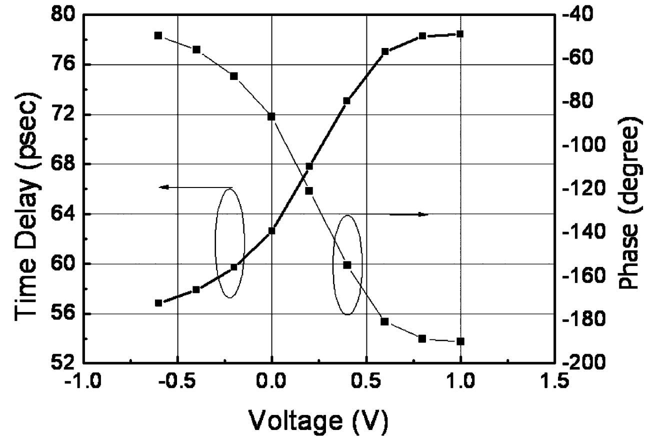

Fig. 3. Measured time delay over the control voltage from -0.6 V to 1 V at 18 GHz.

frequency. For $\omega \gg \omega_B$, the time delay, T_d, of an artificial LHTL delay line is

$$T_d = \frac{N}{\sqrt{LC_v(V_{cont}) \cdot \frac{1}{\omega^2}}} \tag{1}$$

where N is the number of unit cells, L is the inductance, and C_v is the capacitance of the MOS varactor with the control voltage, V_{cont}. The time delay, T_d, varies with the control voltage, V_{cont}. The characteristic impedance, Z_0, is equal to that of the RHTL and can be expressed as follows:

$$Z_0 = \sqrt{\frac{L}{C_v(V_{cont})}}. \tag{2}$$

For minimum reflection around 20 GHz, the inductance and capacitance must be chosen to satisfy (2), 0.4 nH, and 1.256 pF at 0 V, respectively.

III. Measurement Results

Fig. 2 shows a die photograph of the fabricated variable delay line. The chip size, including the pads, is 410 μm$\times$ 640 μm. The delay lines were measured with RF probes and a short-open-load-thru calibration up to the probe tips to measure the S parameter. For the measurements, we used an Agilent 8510C vector network analyzer and a Cascade Microtech probe station. Fig. 3 shows the measured time delay and phase shift over the control voltage from -0.6 V to 1 V at 18 GHz. We achieved a time delay ranging from 56.8 psec to 76.4 psec. Fig. 4 plots the measured input return losses. The input return losses are greater than 10 dB from 18 to 22 GHz. Fig. 5 shows the measured insertion losses. The overall insertion losses ranged from 8 to 13 dB from 18 to 22 GHz. The losses are mainly due to the RF loss of the resistor for the varactor bias. To compare the results with other recently published variable LHTLs, a figure of merit (FOM) is calculated [12]. The measured FOM is 10.9°/dB at 18 GHz as shown in Fig. 6. This result is 0.9°/dB better than the published FOM of 10°/dB at 17 GHz, in high frequency region above 10 GHz [14]. The measured time delay results of the

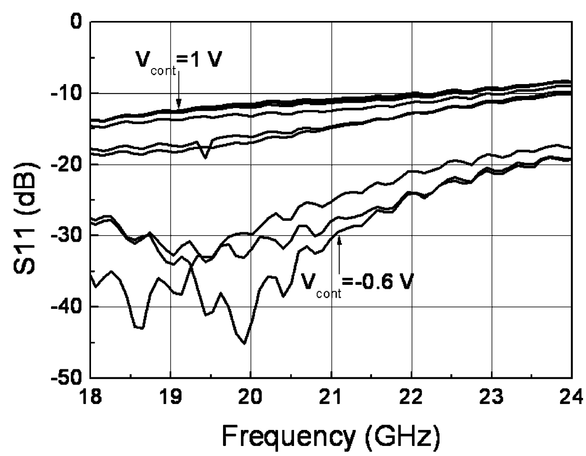

Fig. 4. Measured input return losses in relation to the varying varactor control voltage bias from -0.6 V to 1 V with 0.2 V step.

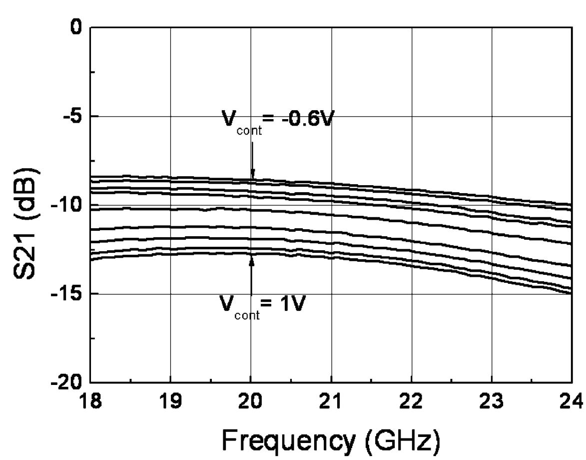

Fig. 5. Measured insertion losses in relation to the varying varactor control voltage bias from -0.6 V to 1 V with 0.2 V step.

RHTL with the same length as the LHTL are shown in Fig. 7 together with the measured time delay results of the LHTL. The time delay is about 30 times longer than that of a traditional RHTL with the same length at 18 GHz. The time delay of the RHTL is constant; in contrast, as shown in (1), the time delay of

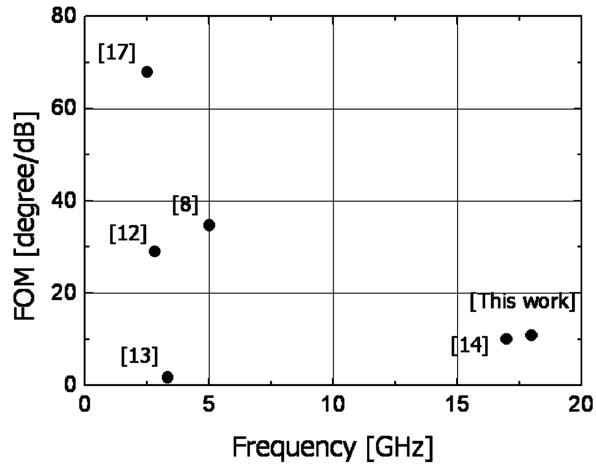

Fig. 6. Comparison of measured FOM with other recently published variable LHTLs.

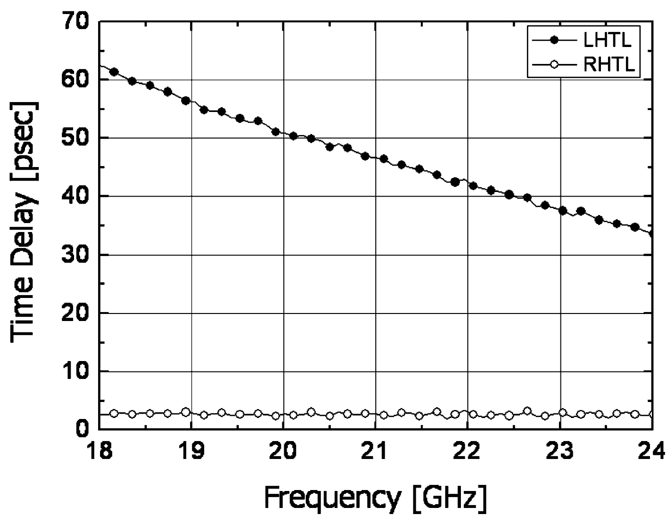

Fig. 7. Measured time delays of delay lines based on an artificial LHTL and a traditional microstrip RHTL.

the LHTL decreases as the frequency increases. The measured 5% time delay deviation is about 0.5 GHz from 18 to 24 GHz. Thus, although the delay line is compact and variable, narrow bandwidth signals must be applied to avoid signal distortion at the output.

IV. Conclusion

We used, for the first time, CMOS technology to demonstrate a K-band voltage controlled delay line based on an artificial LHTL with cascaded MOS varactors and shunt inductors. The line's compact size and variability, as well as the absence of any power consumption, are key advantages for narrowband applications.

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