An Output Matching Technique for a GaN Distributed Power Amplifier MMIC Using Tapered Drain Shunt Capacitors

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***Abstract*—This letter proposes an effective output matching technique using drain shunt capacitors with tapered capacitance values for a GaN distributed power amplifier MMIC to simultaneously obtain optimum load impedance for maximum output power of each transistor and phase velocity balance between input and output artificial transmission lines as well as length reduction of the transmission lines. To support its plausibility, a 2–6 GHz 10 W distributed power amplifier MMIC is designed and fabricated using a 0.25 μm GaN HEMT process of WIN Semiconductors. Measurement of the S parameters and CW output power demonstrates successful operation of the proposed technique in the design frequency range.**

***Index Terms*—Distributed power amplifier (DPA), GaN, HEMT, MMIC, tapered drain shunt capacitors.**

I. Introduction

With the advent of remote-controlled improvised explosive devices, battlefield environments have changed dramatically and a new application field of communication jammers has formed. The new threats should be jammed in the direct surroundings of the unit to be protected, which requires the jammers to operate in a wideband and high-power mode. A GaN high electron mobility transistor (HEMT) on a SiC substrate, which has garnered attention as a next generation semiconductor device and has been actively used in electronic warfare applications, has a wider bandgap than those of conventional Si and GaAs devices. Its wider bandgap of 3.4 eV is associated with high breakdown electric field of 3.3 MV/cm and high saturated electron velocity of 2.5×10^7 cm/s yielding high current density, and its high-power operation benefits from high thermal conductivity of 4.5 W/cm-K, thanks to the SiC substrate [1], [2]. These electrical and thermal properties give rise to higher power density per unit gate width, which provides the GaN HEMT with larger output impedance at the same output power. Finally, the GaN HEMT provides remarkable benefits for wideband power amplifiers as well as communication jammers.

Previously published in the literatures, wideband high-power amplifiers have been implemented using various matching techniques such as reactive filter synthesis [3], a distributed configuration [4], and resistive matching circuits [5], [6]. The reactive filter synthesis and resistive matching techniques have some limitation in extending the bandwidth (BW) of the power amplifiers and cannot obtain good return loss in a wide frequency range. A distributed power amplifier has clear advantages in terms of its return loss and bandwidth, but shows weak points in requiring large area for the circuit implementation and additional circuit tuning for phase velocity balance between input and output transmission lines which affects linear gain performance.

This letter presents an output matching technique to reduce the above disadvantages effectively in designing a GaN nonuniform distributed power amplifier (NDPA) monolithic microwave integrated circuit (MMIC). In the proposed circuit technique, shunt capacitors are intentionally added at drain nodes and their capacitance values are tapered off to simultaneously give optimum load impedance to each transistor at a power-tuned condition and phase velocity balance between input and output artificial transmission lines as well as length reduction of the transmission lines. The proposed technique is demonstrated in a 2–6 GHz 10 W NDPA MMIC using a 0.25 μm GaN HEMT foundry process of WIN Semiconductors [7].

II. Circuit Design

A nonuniform distributed amplifier configuration is chosen to obtain linear gain of more than 10 dB and minimum input return loss of 10 dB. Typically it uses nonuniform output transmission lines for optimum load line of each transistor instead of uniform transmission lines or combines nonuniform output transmission lines with nonuniform-sized transistors with different gate width for better matching and performance [4], [8]. In this work, the former approach is utilized to produce output power of greater than 10 W from 2 to 6 GHz. Using mentioned conventional approaches, we can give each distributed transistor optimal load impedance for maximum output power, but have some difficulty in obtaining phase velocity balance between input and output transmission lines and reducing the length of the transmission lines used in output matching circuits. On the other hand, a conventional distributed amplifier configuration

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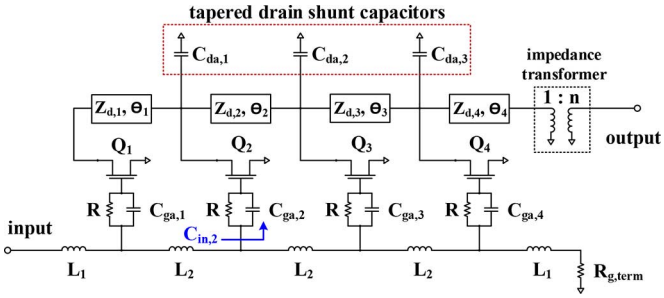

Fig. 1. Schematic circuit of the nonuniform distributed power amplifier MMIC with tapered drain shunt capacitors.

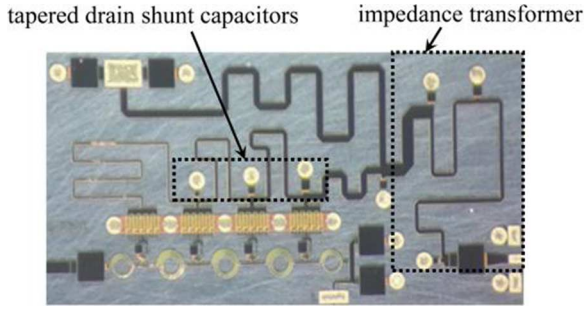

Fig. 2. Chip photograph of the fabricated GaN NDPA MMIC (chip size: 4 mm × 1.9 mm).

with uniform output transmission lines gives equal and nonoptimal output load impedance to all the transistors, thereby not generating maximum output power. The newly presented circuit technique in this work is to properly insert shunt capacitors with tapered capacitance values at the drain nodes of the transistors in the NDPA configuration, thereby obtaining optimal output load impedance for each transistor and phase velocity balance between input and output transmission lines simultaneously.

Fig. 1 shows an NDPA schematic circuit diagram with tapered drain shunt capacitors. The transistors are 0.25 μm GaN HEMTs (10F125, $W_g = 10 \times 125$ μm) from the GaN foundry process of WIN Semiconductors, to which a drain bias voltage of 28 V and drain current of 125 mA per transistor are applied for simulation and measurement. To secure device stability, parallel RC circuits of 300 Ω resistors and capacitors $C_{ga,i}$ (i = 1 to 4) are inserted at the gates of the GaN HEMTs and capacitance values of the inserted capacitors are smoothly increased to compensate the loss due to an input artificial transmission line, as $C_{ga,i} > C_{ga,j}$ (i > j, 1 to 4 in Fig. 1) [9]. The parallel RC circuits attenuate input signals below 2 GHz intentionally and make all RF gate voltages approximately equal at 4 GHz. On the output side, each transistor is matched to power-tuned load impedance using a microstrip line with characteristic impedance of $Z_{d,i}$ and electrical length θ_i, and a drain shunt capacitor $C_{da,i}$ that is intentionally inserted as a tuning element to adjust the phase velocity balance between input and output transmission lines while maintaining optimum load impedance at a power-tuned condition. Design equations for the NDPA with the tapered drain shunt capacitors can be derived as shown below.

First, with the normalized load impedance R_p (Ω·mm) and gate width W_i (i = 1 to 4) of the transistor given, the characteristic impedance $Z_{d,i}$ of the output microstrip line is expressed as (1) [4]. Inductance $L_{out,i}$ of a lumped output inductor forming an output artificial transmission line between the transistors is derived from the phase velocity balance condition and is given as (2) where L_2 is a series inductor to connect the gates of the transistors and $C_{in,i}$ is equivalent input capacitance, seen in front of the parallel RC circuit. Then, to endure high drain current during high-power operation, $L_{out,i}$ is transformed into a short-length microstrip line of $Z_{d,i}$ with θ_i that can be derived as (3), when shunt capacitors are properly added at the drain nodes. Equivalent output capacitance $C_{out,i}$ at the transistor output node, forming the output artificial transmission line together with $L_{out,i}$, includes equivalent drain-source capacitance $C_{ds,i}$ of the transistor at a maximum output power condition and can be obtained simply by inserting the drain shunt capacitor $C_{da,i}$ properly. The required capacitance of the shunt capacitor, $C_{da,i}$, is derived as (4) after some algebraic manipulation. Lastly, optimum load impedance for maximum output power of the rightmost transistor is realized using a wideband impedance transformer which can be size-reduced by an LC ladder network or Π-type network of short microstrip lines and multiple shunt capacitors

$$Z_{d,i} = \frac{R_p(\Omega \cdot mm)}{\sum_{x=1}^{i} W_x} \tag{1}$$

$$L_{\mathrm{out},i} = Z_{d,i}\sqrt{L_2 C_{in,i}} \tag{2}$$

$$\theta_i = \sin^{-1}\left(\frac{\omega L_{\mathrm{out},i}}{Z_{d,i}}\right) \tag{3}$$

$$C_{da,i} = \frac{\cos\theta_i - 1 + \omega^2 L_2 C_{in,i}}{\omega^2 L_{\mathrm{out},i}} - C_{ds,i}. \tag{4}$$

According to simulated results of this work, phase velocity balance between the input and output artificial transmission lines obtained from the tapered drain shunt capacitors improves linear gain of the designed power amplifier by approximately 1.6 dB at 6 GHz and its output return loss by more than 5 dB from 2 to 6 GHz. Typical capacitance variation of 10 % in the tapered capacitors can degrade linear gain by about 0.15 dB at 6 GHz. Also the tapered drain shunt capacitors reduce the length of the microstrip lines connecting the drain nodes of the transistors, thereby decreasing the chip area of this work to 7.6 mm^2 which corresponds to approximately 50 % of that (15.3 mm^2) in [4], although the chip size of a distributed amplifier is mainly determined by lower operating frequencies of the bandwidth.

III. Fabrication and Measurement

A chip photograph of the fabricated NDPA MMIC is shown in Fig. 2 and its size is 4 mm × 1.9 mm. Input transmission lines are implemented with circular spiral inductors and for the output transmission lines, microstrip lines are used to withstand high drain current. The C-L-C Π-type network consisting of three microstrip lines and four shunt capacitors is used for the wideband impedance transformer shown in Fig. 1 and is indicated on the right side of Fig. 2.

Fig. 3 compares measured S-parameter results of the NDPA MMIC with its simulated S-parameter results from 0.5 to 10 GHz. The measurement data shows very good agreement with the simulation data. Input return loss of greater than 10 dB is obtained in a range of 0.5 to 7.7 GHz and output return loss

TABLE I
STATE-OF-THE-ART WIDEBAND GAN POWER AMPLIFIERS

REFERENCES	BW [GHZ]	BW [%]	P_{OUT} [W]	GAIN [DB]	PAE [%]	RETURN LOSS [DB]	CIRCUIT	SIZE [MM^2]
2008 [3]	2-6	100	7-10	14-20 (2-STAGE)	25-30	> 7	MMIC/ REACTIVE	23.04
2009 [4]	1.5-17	168	9-15	> 10	20-38	> 10	MMIC/ DISTRIBUTED	15.3
2010 [5]	1.9-4.3	77	10-15	9-11	50-62	> 4	HYBRID/ RESISTIVE	-
2014 [6]	1-6	143	4	10	> 40	> 5	HYBRID/ RESISTIVE	-
THIS WORK	2-6	100	12.3-14.1	12.8-13.7	27-34	> 10	MMIC/DISTRIBUTED	7.6

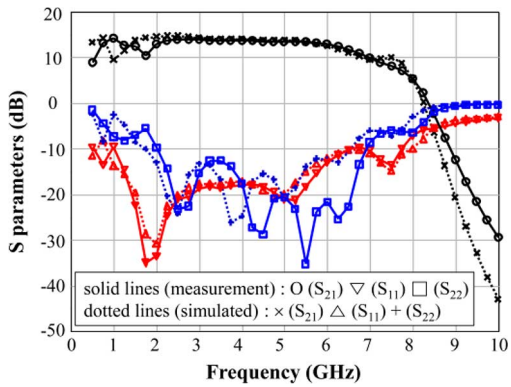

Fig. 3. Comparison of simulated and measured S-parameter results of the fabricated NDPA MMIC.

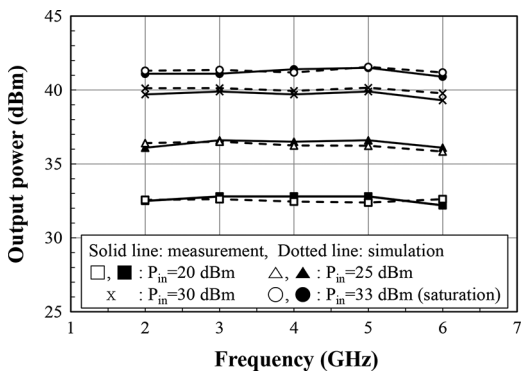

Fig. 4. Measured and simulated CW output power performance with the frequency of the NDPA MMIC with tapered drain shunt capacitors when input power changes.

is larger than 10 dB from 2 to 7 GHz. Flat linear gain S_{21} of larger than 10 dB is measured from 0.5 to 7 GHz. The measured data shows the gain is maintained above 10 dB at 6 GHz as the gain improvement of 1.6 dB is predicted by the simulation. In the frequency range of 2 to 6 GHz, S_{21} is measured to be 12.8–13.7 dB. The proposed output matching technique also improves the output return loss by 5 dB or more.

Fig. 4 shows measured continuous wave (CW) output power in 2 to 6 GHz with input power of 20, 25, 30, and 33 dBm (power saturation condition), and compares it with simulated output power. The fabricated NDPA MMIC shows flat saturated output power of 40.9–41.5 dBm (12.3–14.1 W) and a maximum PAE of 27–34 % from 2 to 6 GHz. The linear and power measurement results are in very good agreement with their counterparts of the simulation.

Comparison between the performance of this work and wideband power amplifiers with the-state-of-the-art results is summarized in Table I. Compared with the previous MMIC results, the proposed output matching technique can provide better input and output return loss than [3], and reduce the chip area of the NDPA MMIC into much smaller area than the chip area (5.54 mm × 2.77 mm) in [4].

IV. CONCLUSION

The 10 W GaN distributed power amplifier MMIC operating from 2 to 6 GHz, to which the new output matching technique using tapered drain shunt capacitors is effectively applied for simultaneous achievement of the optimum power-tuned load impedance for each transistor and phase velocity balance between the input and output artificial transmission lines, is successfully demonstrated using the 0.25 μm GaN HEMT foundry process of WIN Semiconductors. The measured flat gain of 12.8–13.7 dB, good return loss of larger than 10 dB, saturated output power of 40.9–41.5 dBm, and PAE of 27–34% from 2 to 6 GHz support the plausibility of the proposed technique well.

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