4–20 GHz GaAs True-Time Delay Amplifier MMIC

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***Abstract*— A wideband amplifier with a fine control of the true-time delay (TTD) has been successfully implemented using a commercial 0.5-μm GaAs pHEMT monolithic microwave integrated circuit (MMIC) process. The proposed circuit effectively combines switching elements into an artificial transmission line structure in a distributed amplifier to achieve an adjustable TTD which enables time delay control with gain in a wider band than other GaAs-based TTD circuits. The TTD amplifier MMIC achieves a controllable delay of 9 ps, a gain of 9 to 2 dB, and a typical return loss of more than 10 dB from 4 to 20 GHz. The proposed TTD amplifier can be effectively integrated into a multifunction chip based on GaAs semiconductors for wideband active electronically scanned array or phased array systems.**

***Index Terms*— Active electronically scanned array (AESA), distributed amplifier (DA), GaAs pHEMT, monolithic microwave integrated circuit (MMIC), true-time delay (TTD).**

I. Introduction

BEAMFORMING such as beam steering and beam shaping in an active electronically scanned array (AESA) is accomplished by adjusting phases and magnitudes of the transmit/receive signals at each array element. For a wideband sensing system such as a synthetic aperture radar (SAR) and an electronic warfare system, a wider signal bandwidth and a larger array antenna are required to achieve a higher spatial beam resolution. The beam of a conventional wideband AESA has been steered using phase shifters, and tends to squint with the frequency [1]. Therefore, the AESA with a large array size and a wide channel bandwidth requires a true-time delay (TTD) device as an essential beam steering element to prevent the beam squint [2].

Various approaches such as optical or electrical delay lines can be used to obtain the TTD. In a microwave region, microelectromechanical system (MEMS) and monolithic microwave integrated circuit (MMIC) technologies have enabled us to obtain a much finer TTD in a much smaller form factor [1]. Recently, Si- and GaAs-based integrated TTD devices which are advantageous in the design of a multifunction chip including functions of phase shift (or time delay), attenuation (or amplification), and switching have been reported, but suffer from a relatively large insertion loss depending on a circuit configuration [3]–[5].

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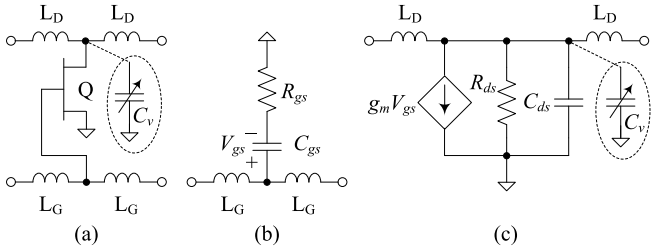

Fig. 1. (a) Schematic circuit of a unit cell of the DA and its equivalent circuits at (b) gate side and (c) drain side. The TTDA is implemented by adding C_v to the drain node of the DA unit cell.

This letter proposes a new TTD amplifier that can provide a tunable time delay together with a gain in 4–20 GHz. The proposed circuit effectively combines a distributed amplifier (DA) with a tunable artificial transmission line which is composed of a cascade of series inductance and shunt capacitance. The tunable TTD is achieved by changing the shunt capacitance of the output transmission line in the DA through switch elements. The feasibility of the proposed circuit is demonstrated using a commercial 0.5-μm GaAs MMIC process.

II. Circuit Design

A TTD amplifier (TTDA) is based on a DA topology that has advantages in a flat gain and good return loss over a wide frequency range, compared with other reactive amplifier structures. The principle of operation and design considerations of a DA have been well described in the literature [6]. In input and output sections of a DA, the inductors of L_G and L_D combine with the intrinsic elements of the transistor to act as input and output artificial transmission lines, as shown in Fig. 1. Therefore, the DA has a flat and low-pass response with a very high cutoff frequency because it absorbs frequency limiting gate and drain capacitances into constituent elements of a transmission line.

Applying the Bloch–Floquet theorem to the circuit in Fig. 1(c), the cutoff frequency f_c, group delay τ_g, and characteristic impedance Z_C are found as follows [7]:

$$f_c = \frac{1}{\pi\sqrt{2L_D C_{\rm ds}}} \tag{1}$$

$$\tau_g = \frac{\sqrt{2L_D C_{\rm ds}}}{\sqrt{1-\frac{\omega^2 L_D C_{\rm ds}}{2}}} = \frac{1}{\pi f_c\sqrt{1-\left(\frac{f}{f_c}\right)^2}} \tag{2}$$

$$Z_C = Z_0\sqrt{1-\left(\frac{f}{f_c}\right)^2}. \tag{3}$$

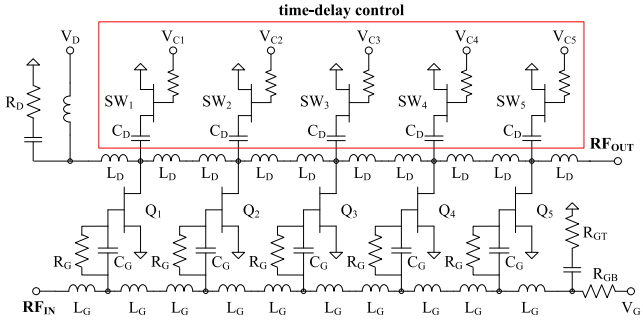

Fig. 2. Schematic circuit of the TTD amplifier with a time delay control circuit.

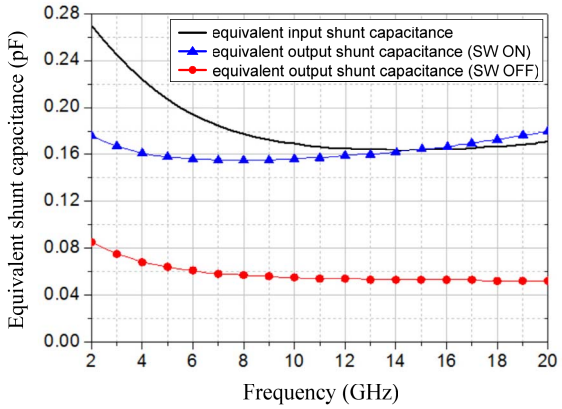

Fig. 3. Simulated equivalent shunt capacitances of input and output transmission lines when the switch transistor is ON or OFF.

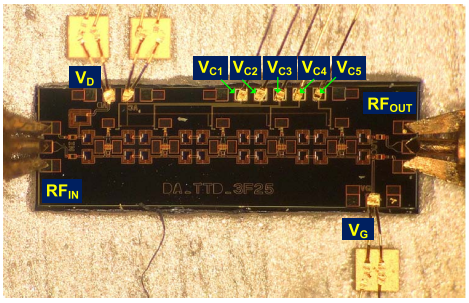

Fig. 4. Photograph of the TTDA MMIC (dimensions of 3 mm × 1 mm).

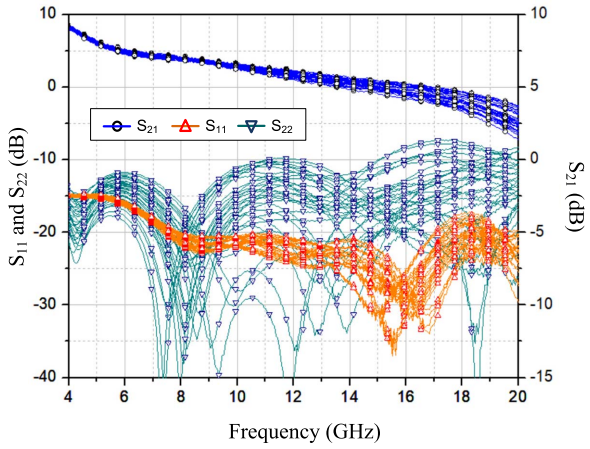

Fig. 5. Measured S-parameter results of the fabricated TTDA MMIC with the 32 switching states.

The equations of (2) and (3) are approximated to $\tau_g \approx 1/\pi f_c$ and $Z_C \approx Z_0$ when the operating frequency f is well below the cutoff frequency f_c. In the TTDA structure, a time delay which is inversely proportional to f_c can be adjusted by the variable shunt capacitance C_v of the drain transmission line.

A TTDA MMIC is designed using a 0.5-μm InGaAs pHEMT device. The periphery of transistors in the TTDA is determined by the cutoff frequency of an artificial transmission line and the required linear gain. In this letter, a 4×30 μm transistor is used and extracted intrinsic elements of its equivalent device model are $C_{\rm gs} = 0.3$ pF, $R_{\rm gs} = 8.8$ Ω, $C_{\rm ds} = 0.027$ pF, and $R_{\rm ds} = 688$ Ω at 14 GHz. If the input and output impedances of the amplifier are set to 50 Ω, the cutoff frequency of the DA which is mainly determined by the gate line is estimated to be 21.2 GHz, and the upper frequency limit for a flat gain response is 17 GHz ($= 0.8 f_c$). The DA cutoff frequency can be increased through the insertion of series-connected coupling capacitors at the gates of the transistors, although the linear gain of the DA degrades a little. The coupling capacitors also play a role as a stabilizer when they are connected in parallel with resistors.

The conventional DA design experimentally tunes the inductance or electrical length of the gate and drain lines to obtain a phase velocity balance between them. In the previous study, we proposed a circuit technique inserting shunt capacitors at the drain nodes to simultaneously achieve an optimal load impedance and a phase velocity balance between input and output transmission lines in a DA configuration [8]. In this letter, a TTDA is implemented using shunt capacitors and switching transistors as time delay control elements at the drain nodes of the transconductance amplifying transistors. Since $C_{\rm gs}$ is much larger than $C_{\rm ds}$ and the cutoff frequency of a drain transmission line is higher than that of a gate transmission line, shunt elements at the drain nodes enable obtaining the time delay control and the phase velocity balance simultaneously.

Fig. 2 shows a schematic circuit diagram of the TTDA with a time delay control circuit of dc blocking capacitors (C_D) and shunt-connected switch transistors (SW$_n$). A parallel network of R_G and C_G at the gate of each transistor extends the cutoff frequency of the input artificial transmission line and stabilizes the TTDA unconditionally. The value of C_G is set not more than the value of $C_{\rm gs}$, and R_G has a little high value to avoid affecting the capacitive coupling through C_G. The C_G and R_G in this letter are 0.25 pF and 100 Ω, respectively. The input equivalent capacitance of the C_G and the 4×30 μm amplifying transistor (Q_n) reduces to 0.16 pF, which raises the cutoff frequency to 39 GHz.

In the time delay control circuit, when a switch transistor is ON, an equivalent shunt capacitance of the unit cell of the output transmission line changes from $C_{\rm ds} + C_{\rm SW\_OFF}$ to $C_{\rm ds} + C_D$. If the C_D is set to 0.11 pF, the equivalent shunt capacitance of the output transmission line becomes very similar to that of the input transmission line when the switch is ON, as shown in Fig. 3. Depending on the ON/OFF state of

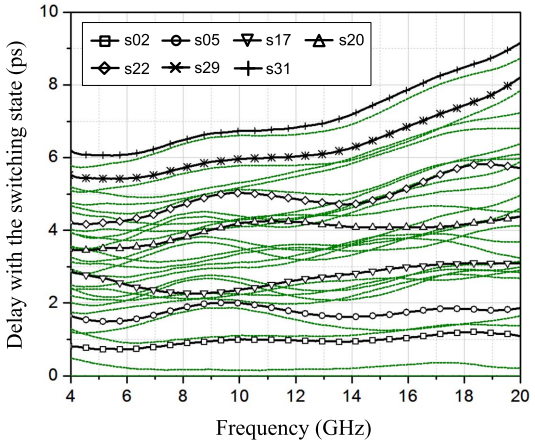

Fig. 6. Measured relative delay of the fabricated TTDA MMIC with the 32 switching states. (Lines marked with symbols indicate representative states).

TABLE I
COMPARISON WITH PREVIOUSLY REPORTED DESIGN

Ref.	Technology	Bandwidth (GHz)	Resolution (ps)	Maximum Delay (ps)	Gain (dB)
[2]	0.18 μm BiCMOS SiGe	2–15	4	64	7 to 10
[3]	HMIC on RT/Duroid 5880*	0.5–3	Continuous†	-	6.5 to 12.5
[4]	0.2 μm pHEMT GaAs	2–20	2.2	145	-7 to -25
This work	0.5 μm pHEMT GaAs	4–20	≤ 1	9	2 to 9

*Amplification is based on the Agilent ATF-36077 HEMT
†Maximum phase shift of 35° at 3.5 GHz

the switch transistor, the equivalent output shunt capacitance changes by 0.105 pF at 12 GHz, and with the time delay control circuit the TTDA achieves a maximum TTD change of 9 ps. A photograph of the fabricated TTDA MMIC is shown in Fig. 4. The chip occupies an area of 3 mm × 1 mm.

III. MEASUREMENT

The TTDA MMIC is nominally biased at a drain–source voltage of 3 V and a drain current of 78 mA. Fig. 5 shows the on-wafer measured S_{21}, S_{11}, and S_{22} of the fabricated TTDA MMIC with all 32 switching states. The small signal gain is 9 to 2 dB, the input return losses are better than 15 dB and the output return losses are better than 10 dB, excluding a few switching states, from 4 to 20 GHz. The maximum gain variation with the switching states is about 2 dB at 20 GHz.

The ON/OFF states of the five switches can be represented by binary digits and have a total of 32 states. Fig. 6 shows the measured delay time of the fabricated TTDA MMIC for all 32 states. The reference state (s00) is when all the switches are OFF, and s31 is when all the switches are ON. The delay time of the circuit can be set up to a maximum of 9 ps from 4 to 20 GHz. Some crossings between states in the time delay still remain to be improved through the detail analysis and careful design. The measured performance of our work is compared with previously reported state-of-the-art results in Table I.

IV. CONCLUSION

We proposed a 4–20 GHz GaAs TTDA MMIC with the gain and TTD control over a wide frequency range and demonstrated its feasibility. We utilized a DA topology for the TTDA and added a switch transistor at the drain node of each transistor in the amplifier as a time delay control element. The TTDA showed the controllable delay of maximum 9 ps and the gain of 9 to 2 dB. The proposed TTDA can be used as an amplifier with a tunable TTD function and be effectively integrated into a GaAs multifunction chip for wideband AESA or phased array systems.

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